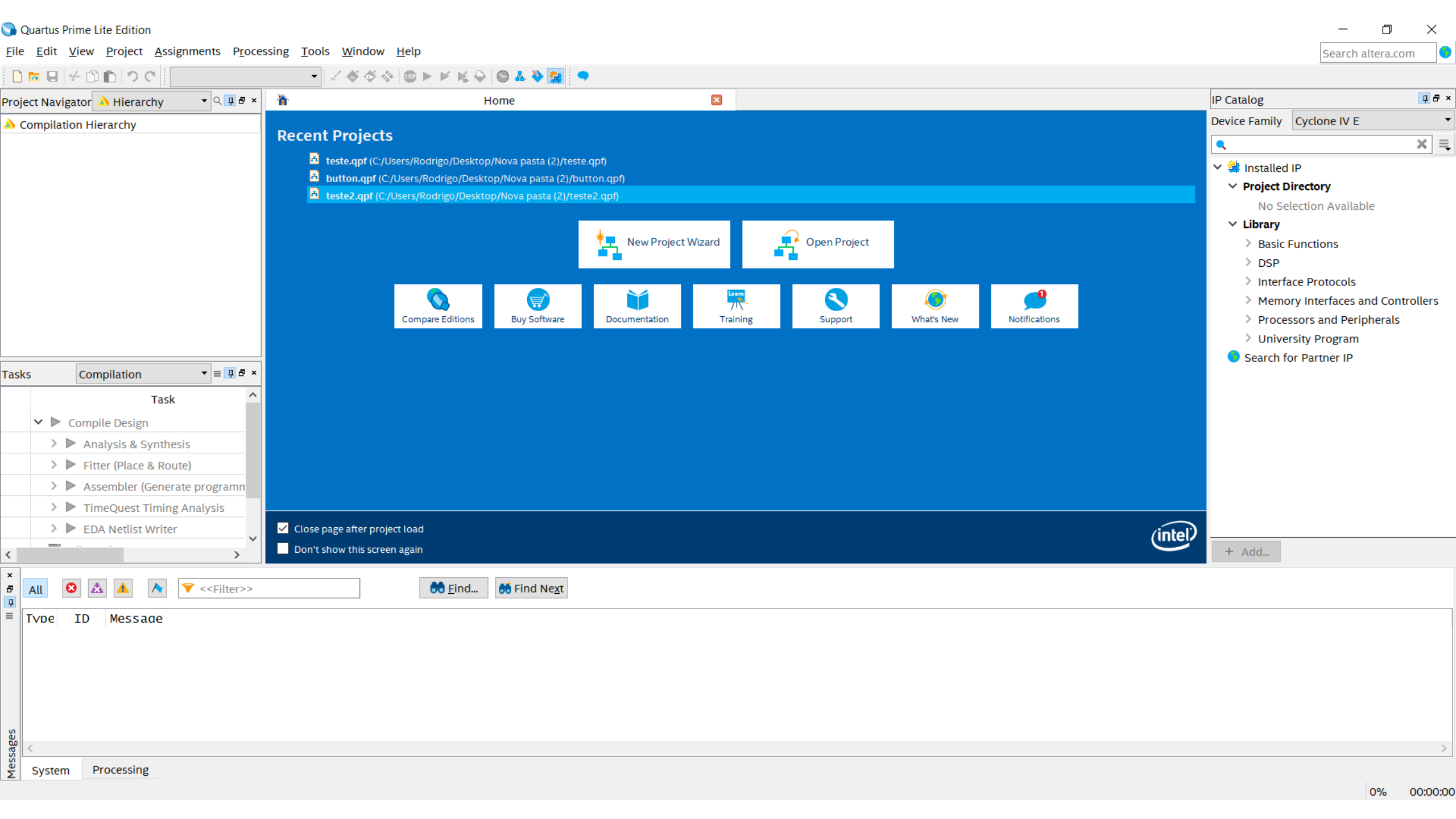
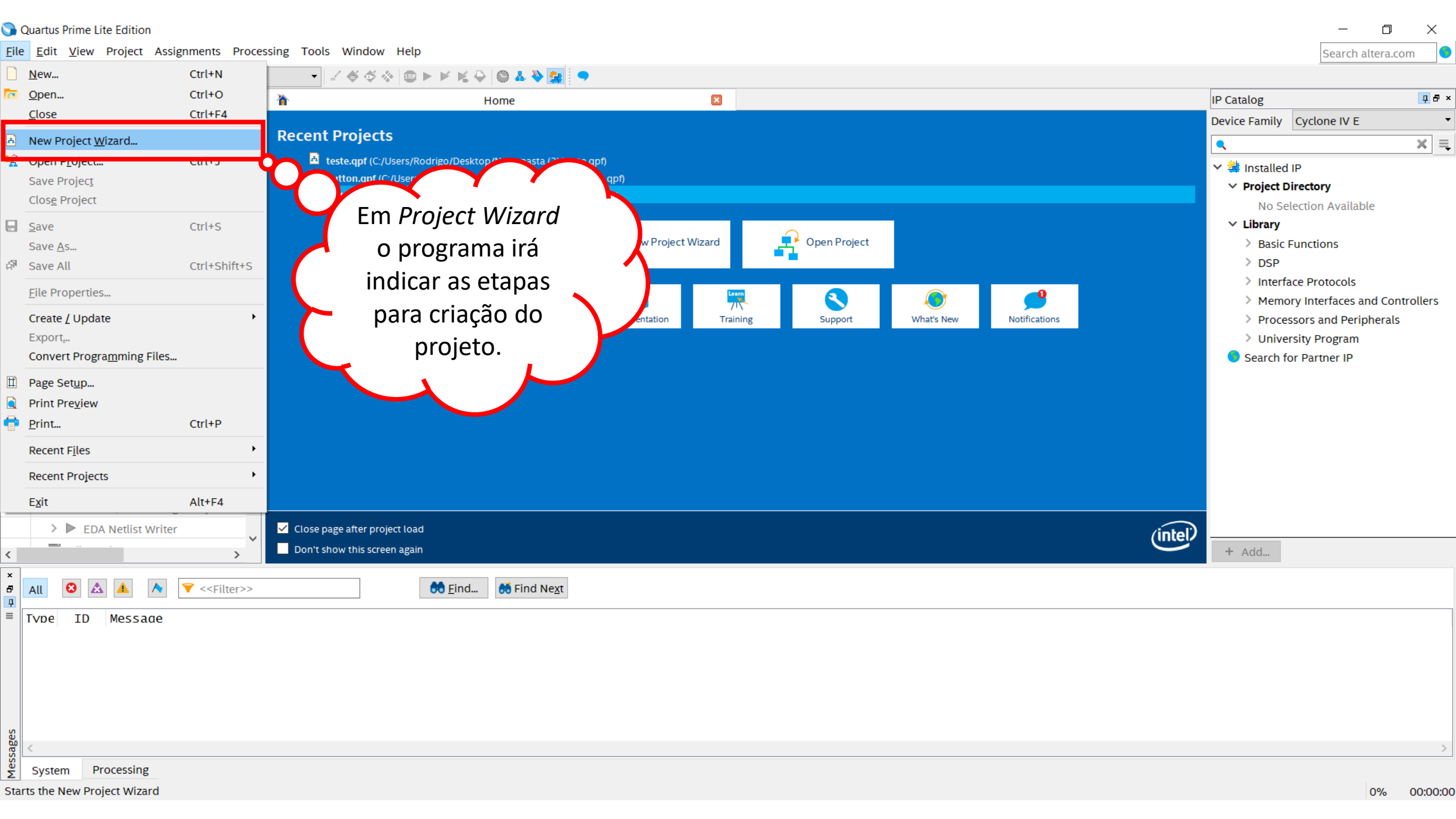
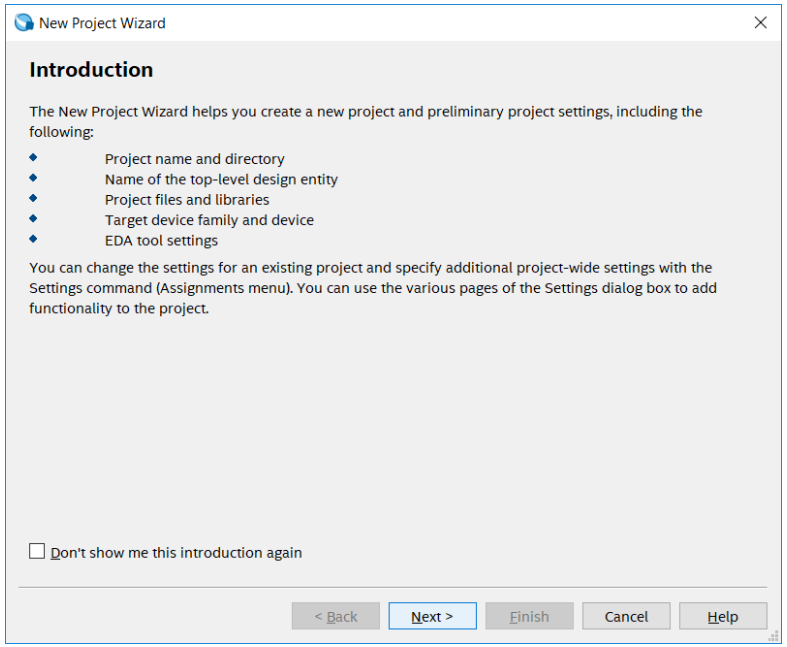
Tutorial Quartus Prime

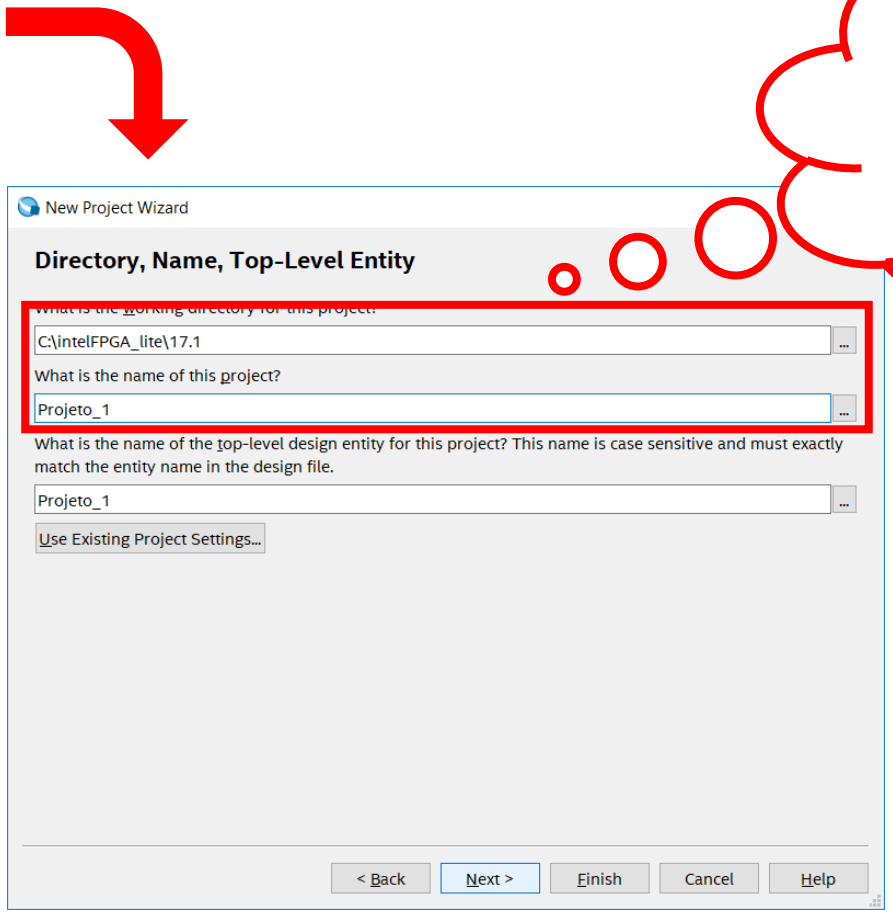
Prof. Rodrigo Rech

V1.0 – CPLD EPM240T100C5

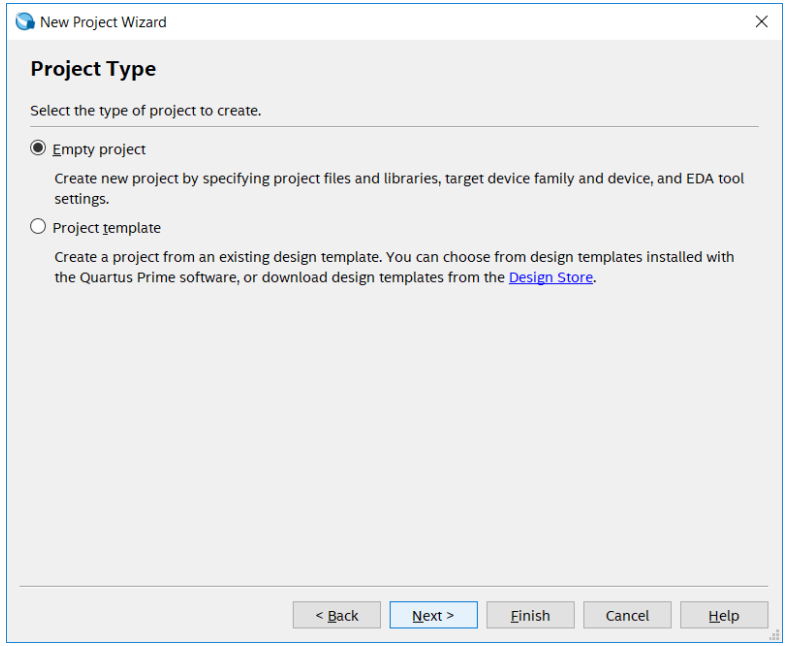

Quartus Prime Lite Edition
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Project Navigator Hierarchy
Compilation Hierarchy
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programn
TimeQuest Timing Analysis
EDA Netlist Writer
Home
Recent Projects
teste.qpf (C:/Users/Rodrigo/Desktop/Nova pasta (2)/teste.qpf)
button.qpf (C:/Users/Rodrigo/Desktop/Nova pasta (2)/button.qpf)
teste2.qpf (C:/Users/Rodrigo/Desktop/Nova pasta (2)/teste2.qpf)
New Project Wizard
Open Project
Compare Editions
Buy Software
Documentation
Training
Support
What's New
Notifications
Close page after project load
Don't show this screen again
IP Catalog
Device Family Cyclone IV E
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
Messages
System
Processing
0%
00:00:00

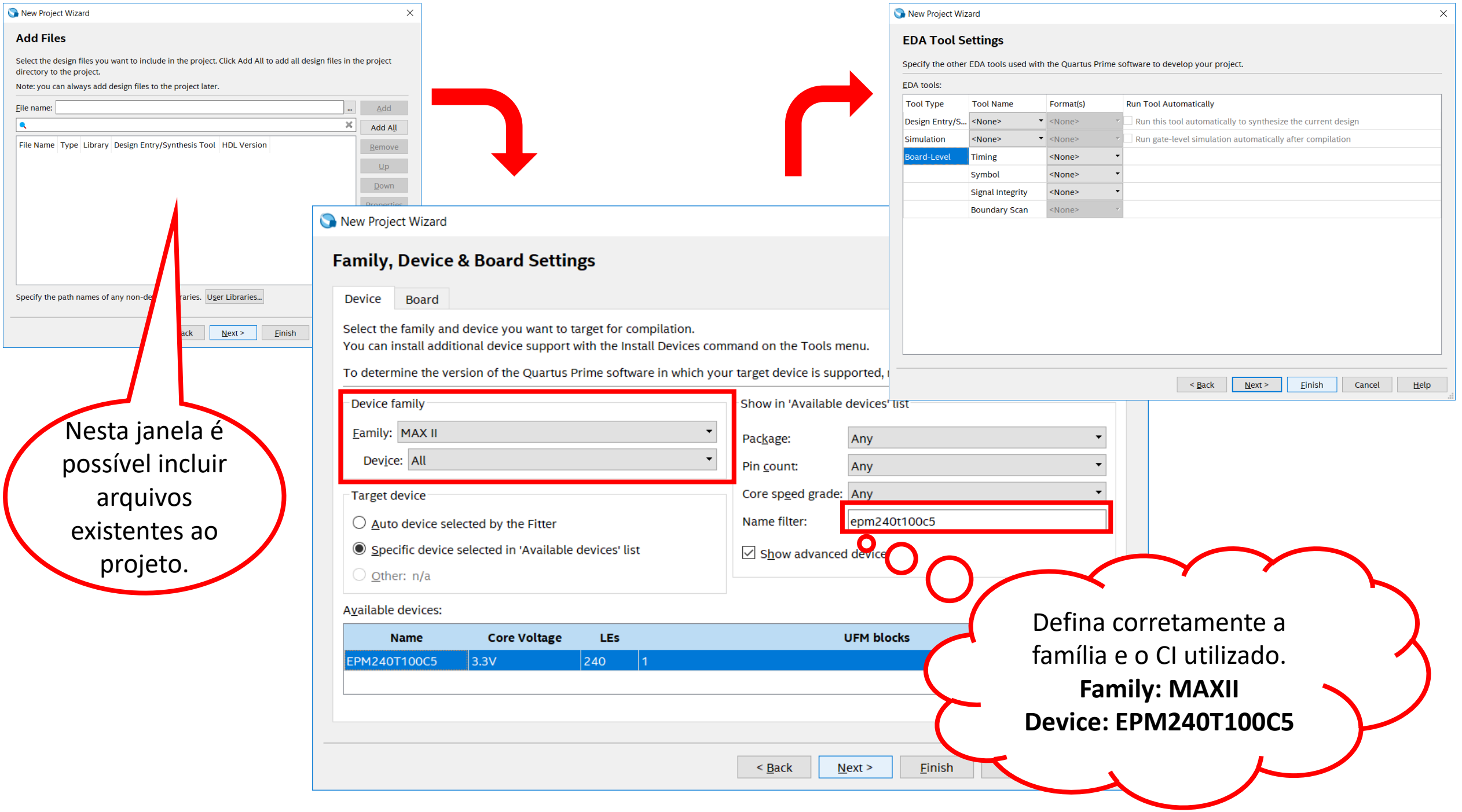

Quartus Prime Lite Edition
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4
Em Project Wizard o programa irá indicar as etapas para criação do projeto.
Home
Recent Projects
teste.qpf (C:/Users/Rodrigo/Desktop/
Open Project
Training
Support
What's New
Notifications
Close page after project load
Don't show this screen again
IP Catalog
Device Family
Cyclone IV E
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
Add...
EDA Netlist Writer
All
<<Filter>>
Find...
Find Next
Type ID Message
Messages
System
Processing
Starts the New Project Wizard
0%
00:00:00

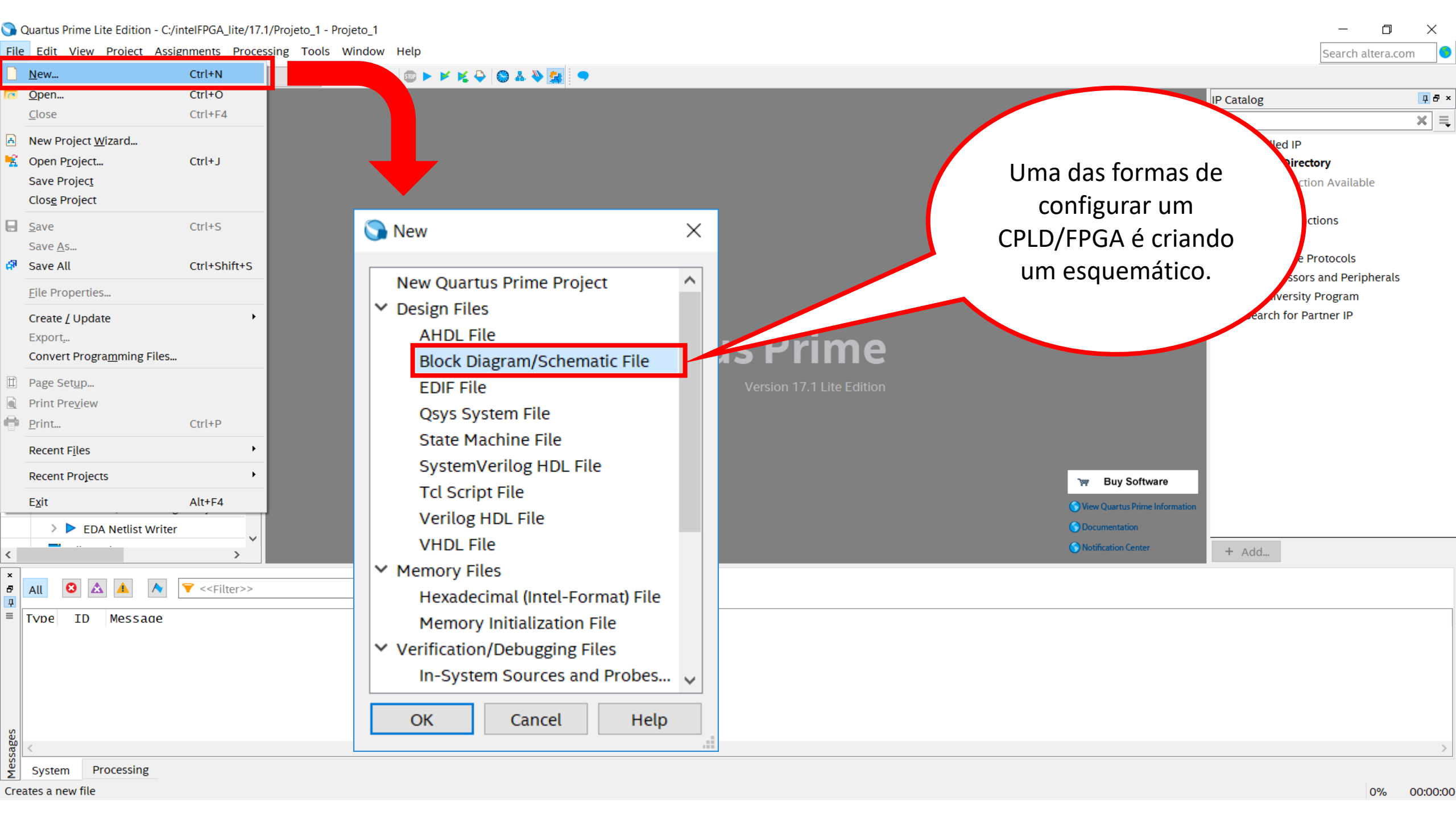


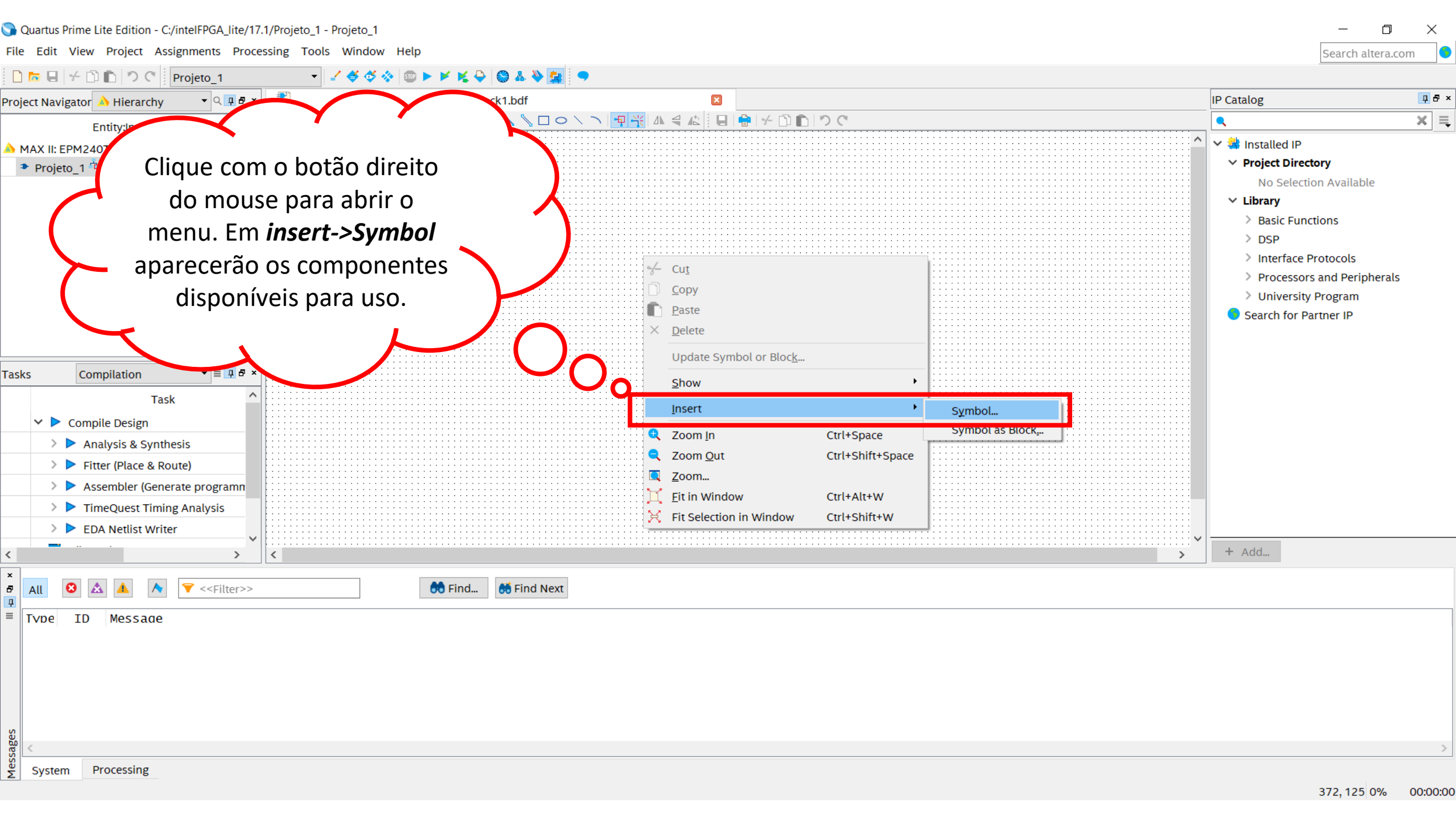


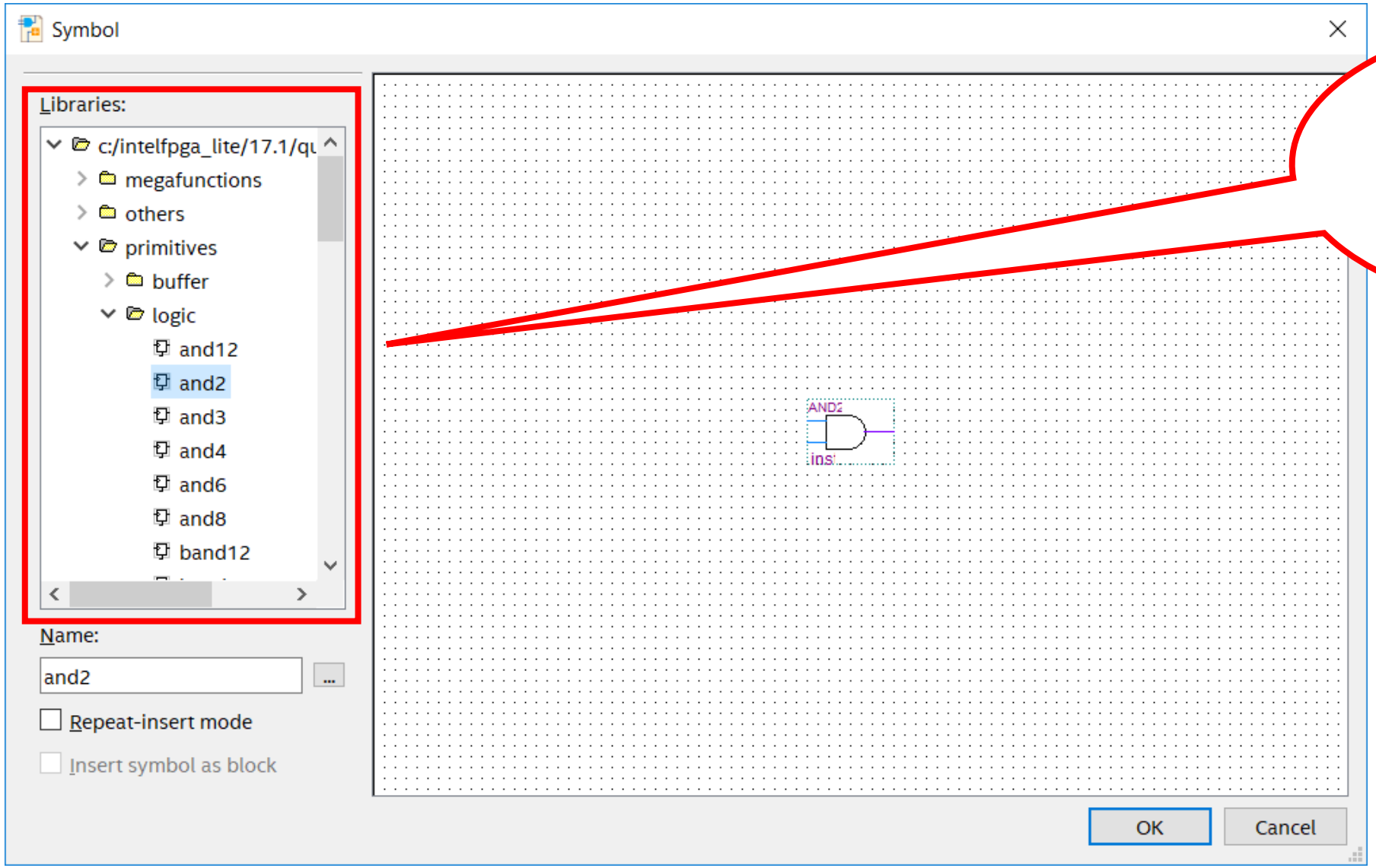
Defina uma pasta de destino e um nome para o Projeto.
Evite utilizar o diretório padrão, crie sua própria pasta em outro local!



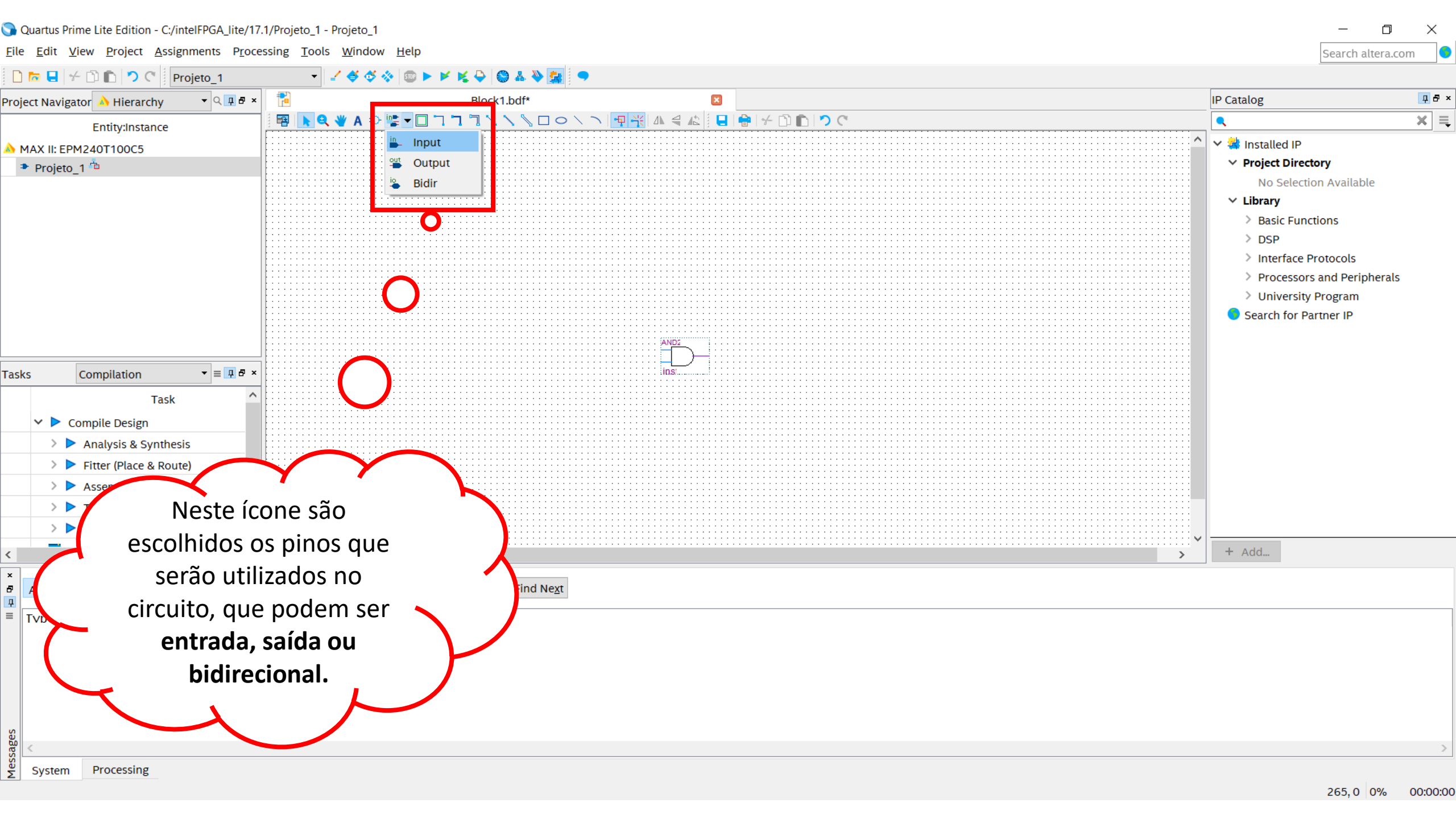

New Project Wizard
Add Files
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
Note: you can always add design files to the project later.
File name:
Add
Add All
Remove
Up
Down
File Name
Type
Library
Design Entry/Synthesis Tool
HDL Version
User Libraries...
Next >
Finish
New Project Wizard
Family, Device & Board Settings
Device
Board
Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.
To determine the version of the Quartus Prime software in which your target device is supported,
Device family
Family: MAX II
Device: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Core speed grade: Any
Name filter: epm240t100c5
Show advanced device
Available devices:
Name
Core Voltage
LEs
UFM blocks
EPM240T100C5
3.3V
240
1
< Back
Next >
Finish
New Project Wizard
EDA Tool Settings
Specify the other EDA tools used with the Quartus Prime software to develop your project.
EDA tools:
Tool Type
Tool Name
Format(s)
Run Tool Automatically
Design Entry/S...
Simulation
Board-Level
Timing
Symbol
Signal Integrity
Boundary Scan
<None>
Run this tool automatically to synthesize the current design
Run gate-level simulation automatically after compilation
< Back
Next >
Finish
Cancel
Help
Nesta janela é possível incluir arquivos existentes ao projeto.
Defina corretamente a família e o CI utilizado.
Family: MAXII
Device: EPM240T100C5

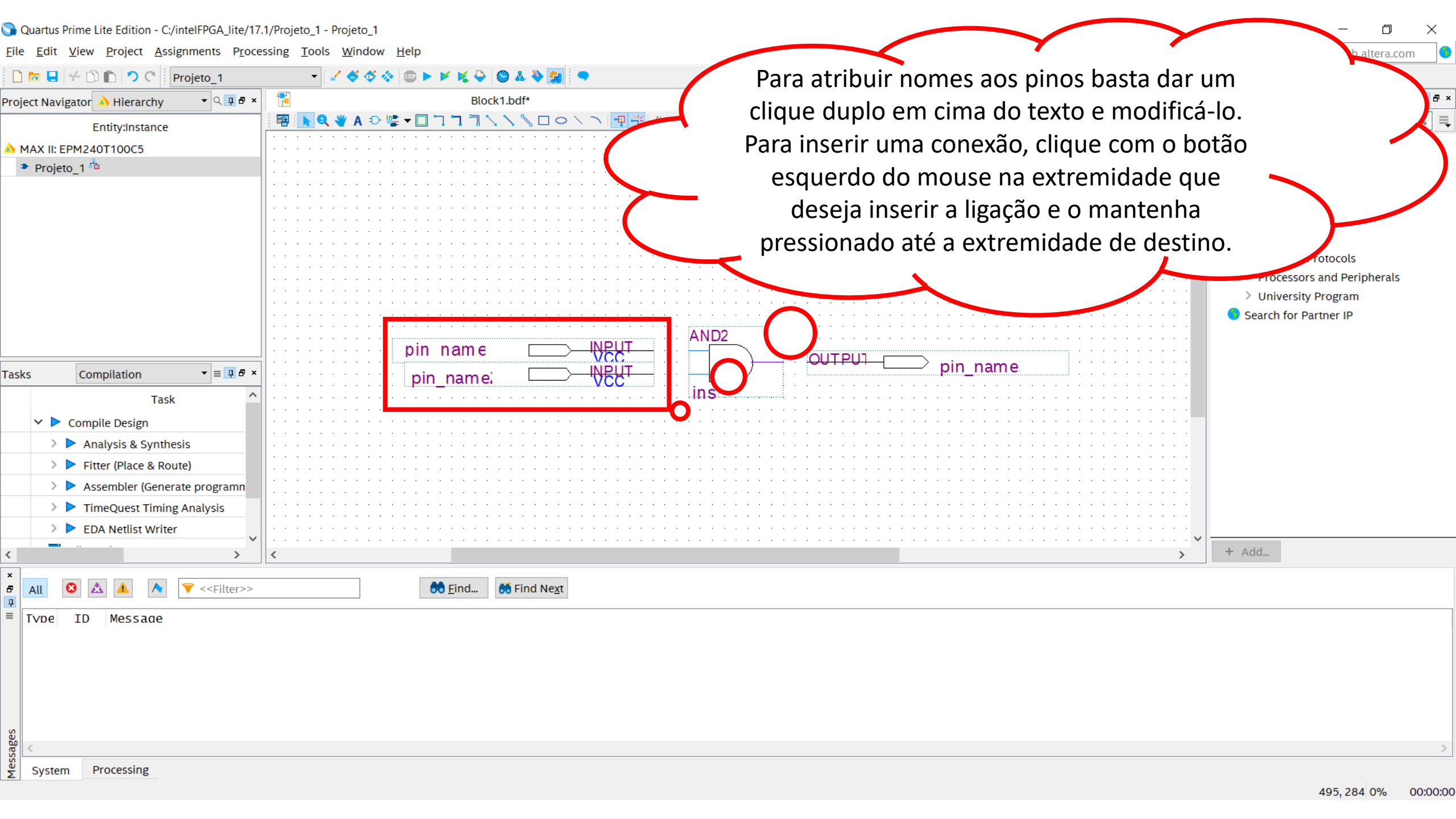

Quartus Prime Lite Edition - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1
File Edit View Project Assignments Processing Tools Window Help
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4
New
New Quartus Prime Project
Design Files
AHDL File
Block Diagram/Schematic File
EDIF File
Qsys System File
State Machine File
SystemVerilog HDL File
Tcl Script File
Verilog HDL File
VHDL File
Memory Files
Hexadecimal (Intel-Format) File
Memory Initialization File
Verification/Debugging Files
In-System Sources and Probes...
OK
Cancel
Help
Uma das formas de configurar um CPLD/FPGA é criando um esquemático.
Version 17.1 Lite Edition
Buy Software
View Quartus Prime Information
Documentation
Notification Center
IP Catalog
Add...
EDA Netlist Writer
All
<<Filter>>
Type ID Message
System
Processing
Creates a new file
0%
00:00:00

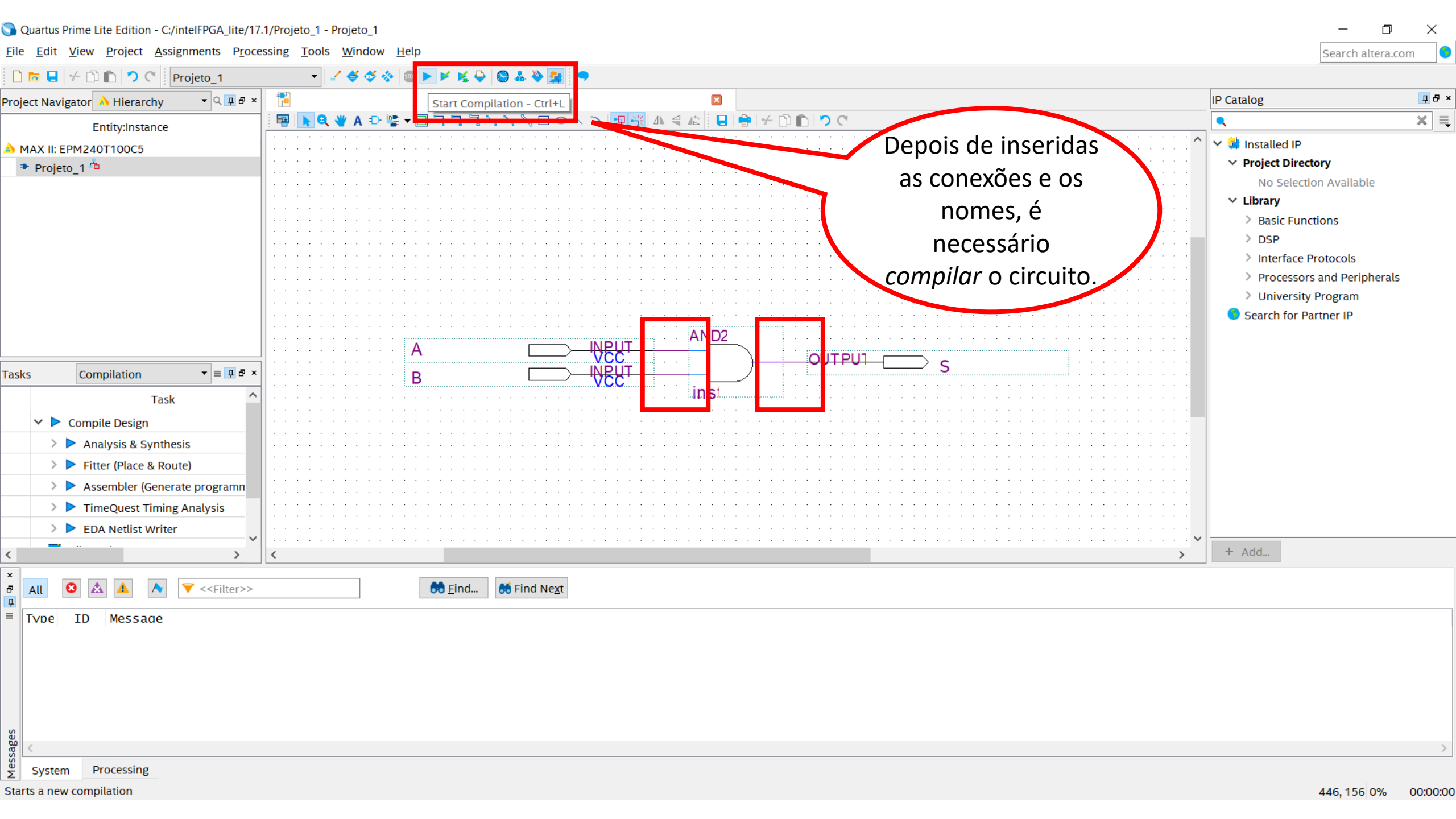

Quartus Prime Lite Edition - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Projeto_1
Project Navigator Hierarchy
MAX II: EPM2407
Projeto_1
Clique com o botão direito do mouse para abrir o menu. Em *insert->Symbol* aparecerão os componentes disponíveis para uso.
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
TimeQuest Timing Analysis
EDA Netlist Writer
Cut
Copy
Paste
Delete
Update Symbol or Block...
Show
Insert
Symbol...
Symbol as Block...
Zoom In Ctrl+Space
Zoom Out Ctrl+Shift+Space
Zoom...
Fit in Window Ctrl+Alt+W
Fit Selection in Window Ctrl+Shift+W
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
Messages
System
Processing
372, 125 0% 00:00:00

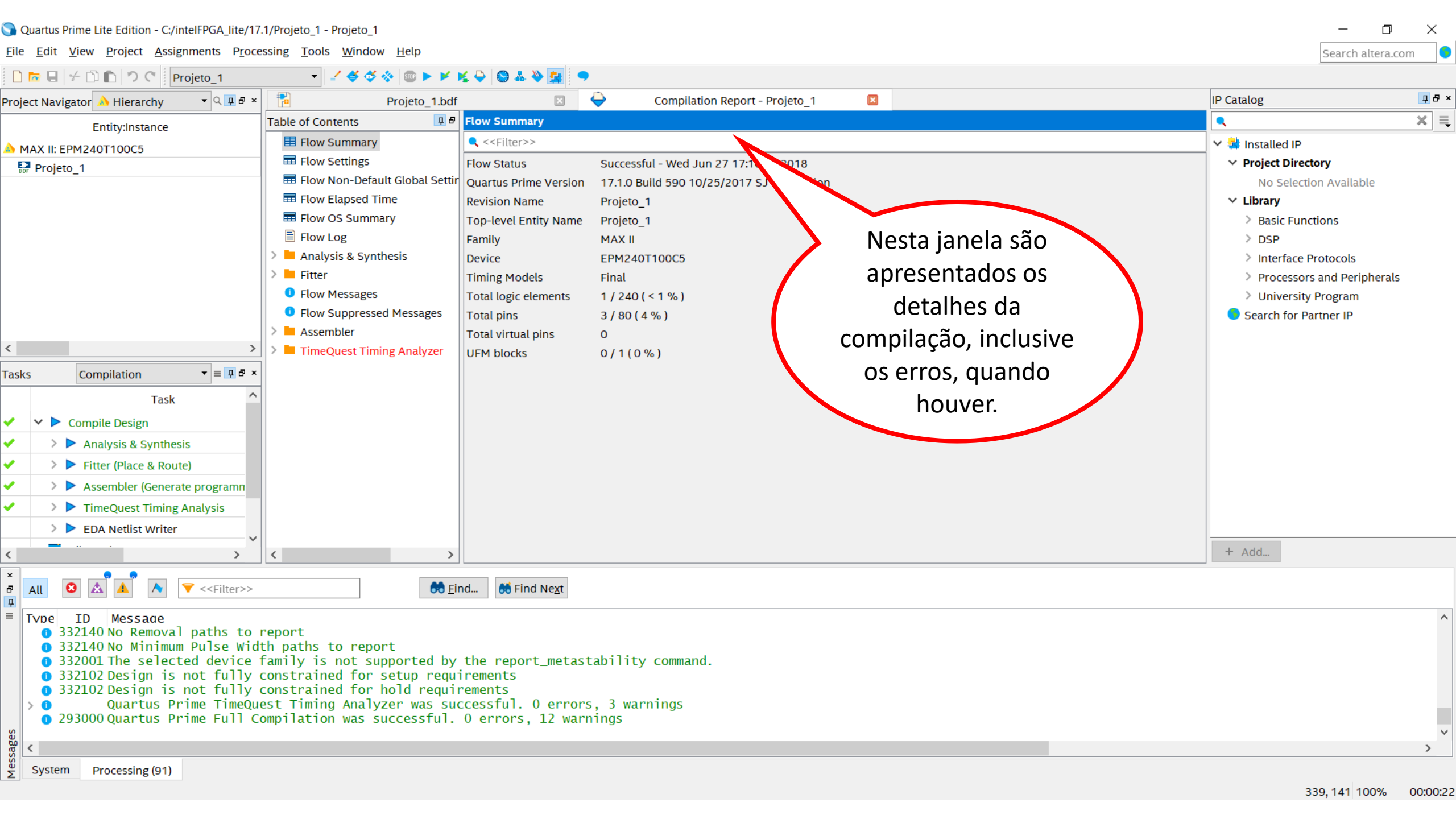


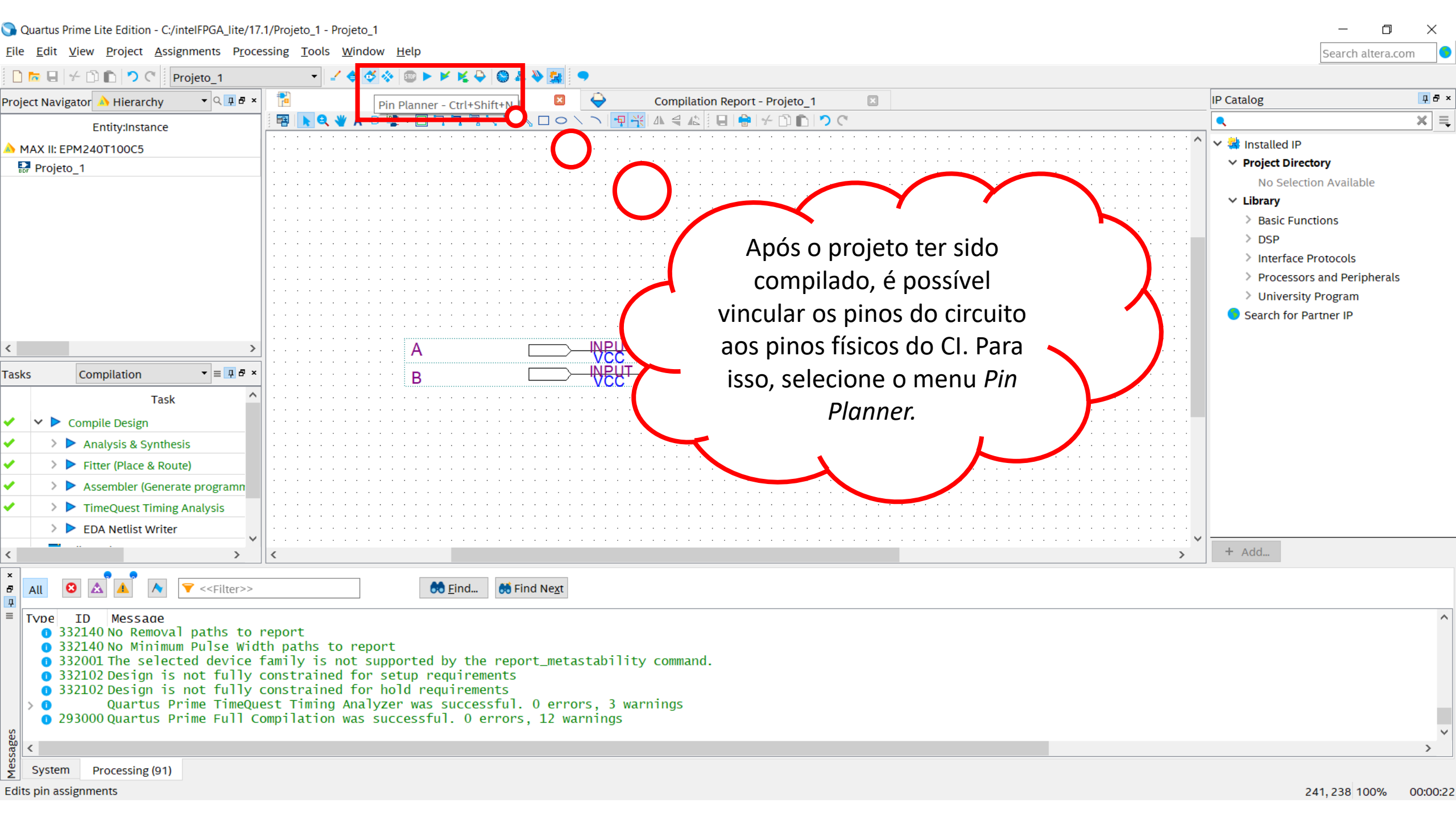
O Quartus possui uma biblioteca bem extensa. Os componentes básicos se encontram na pasta indicada.


Quartus Prime Lite Edition - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Projeto_1
Project Navigator
Hierarchy
Entity:Instance
MAX II: EPM240T100C5
Projeto_1
Block1.bdf*
Input
Output
Bidir
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
Add...
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Find Next
Messages
System
Processing
265, 0
0%
00:00:00
Neste ícone são escolhidos os pinos que serão utilizados no circuito, que podem ser entrada, saída ou bidirecional.


Quartus Prime Lite Edition - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1
File Edit View Project Assignments Processing Tools Window Help
Projeto_1
Project Navigator Hierarchy
Entity:Instance
MAX II: EPM240T100C5
Projeto_1
Block1.bdf*
Para atribuir nomes aos pinos basta dar um clique duplo em cima do texto e modificá-lo. Para inserir uma conexão, clique com o botão esquerdo do mouse na extremidade que deseja inserir a ligação e o mantenha pressionado até a extremidade de destino.
pin_name
INPUT
VCC
pin_name2
INPUT
VCC
AND2
ins
OUTPUT
pin_name
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programn
TimeQuest Timing Analysis
EDA Netlist Writer
Processors and Peripherals
University Program
Search for Partner IP
Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
Messages
System
Processing
495, 284 0%
00:00:00


Quartus Prime Lite Edition - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Projeto_1
Start Compilation - Ctrl+L
Project Navigator Hierarchy
Entity:Instance
MAX II: EPM240T100C5
Projeto_1
Depois de inseridas as conexões e os nomes, é necessário *compilar* o circuito.
A
B
INPUT
VCC
INPUT
VCC
AND2
inst
OUTPUT
S
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
Add...
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
TimeQuest Timing Analysis
EDA Netlist Writer
All
<<Filter>>
Find...
Find Next
Type ID Message
Messages
System
Processing
Starts a new compilation
446, 156 0%
00:00:00


Quartus Prime Lite Edition - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Projeto_1
Project Navigator Hierarchy
Entity:Instance
MAX II: EPM240T100C5
Projeto_1
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programn
TimeQuest Timing Analysis
EDA Netlist Writer
Projeto_1.bdf
Compilation Report - Projeto_1
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settir
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Flow Messages
Flow Suppressed Messages
Assembler
TimeQuest Timing Analyzer
Flow Summary
<<Filter>>
Flow Status Successful - Wed Jun 27 17:1 2018
Quartus Prime Version 17.1.0 Build 590 10/25/2017 SJ
Revision Name Projeto_1
Top-level Entity Name Projeto_1
Family MAX II
Device EPM240T100C5
Timing Models Final
Total logic elements 1 / 240 (< 1 %)
Total pins 3 / 80 (4 %)
Total virtual pins 0
UFM blocks 0 / 1 (0 %)
Nesta janela são apresentados os detalhes da compilação, inclusive os erros, quando houver.
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
+ Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
332140 No Removal paths to report
332140 No Minimum Pulse Width paths to report
332001 The selected device family is not supported by the report_metastability command.
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 3 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 12 warnings
Messages
System
Processing (91)
339, 141 100% 00:00:22

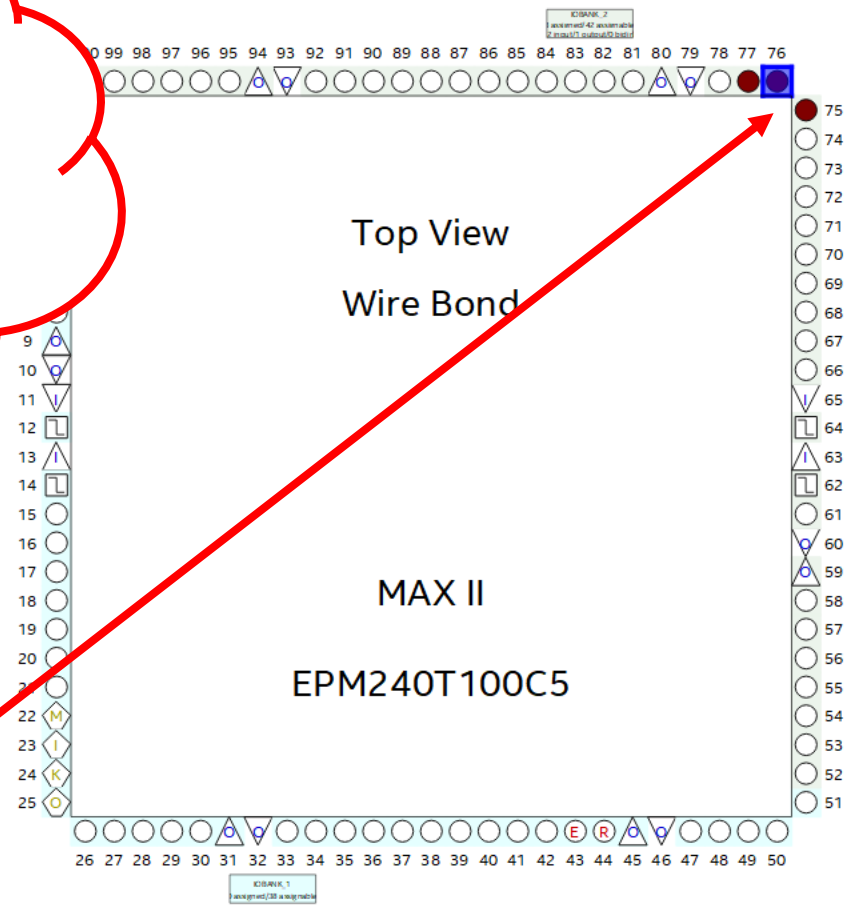

Quartus Prime Lite Edition - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Projeto_1
Project Navigator Hierarchy
Entity:Instance
MAX II: EPM240T100C5
Projeto_1
Pin Planner - Ctrl+Shift+N
Compilation Report - Projeto_1
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
Add...
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programn
TimeQuest Timing Analysis
EDA Netlist Writer
A
B
INPUT
VCC
Após o projeto ter sido compilado, é possível vincular os pinos do circuito aos pinos físicos do CI. Para isso, selecione o menu *Pin Planner.*
All
<<Filter>>
Find...
Find Next
Type ID Message
332140 No Removal paths to report
332140 No Minimum Pulse Width paths to report
332001 The selected device family is not supported by the report_metastability command.
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 3 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 12 warnings
Messages
System
Processing (91)
Edits pin assignments
241, 238 100%
00:00:22

Pin Planner - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1

File Edit View Processing Tools

Search altera.com

Nesta tabela estão os pinos do projeto e a sua localização física. Para atribuir os pinos basta clicar no nome do pino e arrastar até o pino físico desejado.



Report

Groups Report

Tasks

- Early Pin Planning
  - Early Pin Planning...
  - Run I/O Assignment A
  - Export Pin Assignmen
- Pin Finder...
- Highlight Pins
  - I/O Banks
  - Edges
  - Clock Pins

Pin Legend

Symbol	Pin Type
	User I/O
	User assign...
	Fitter assign...
	Unbonded ...
	Reserved pin
E	DEV_OE
R	DEV_CLR
	CLK_n
I	TDI
K	TCK
M	TMS
O	TDO
	VCCINT
	VCCIO
	GNDINT
	GNDIO

Node Properties

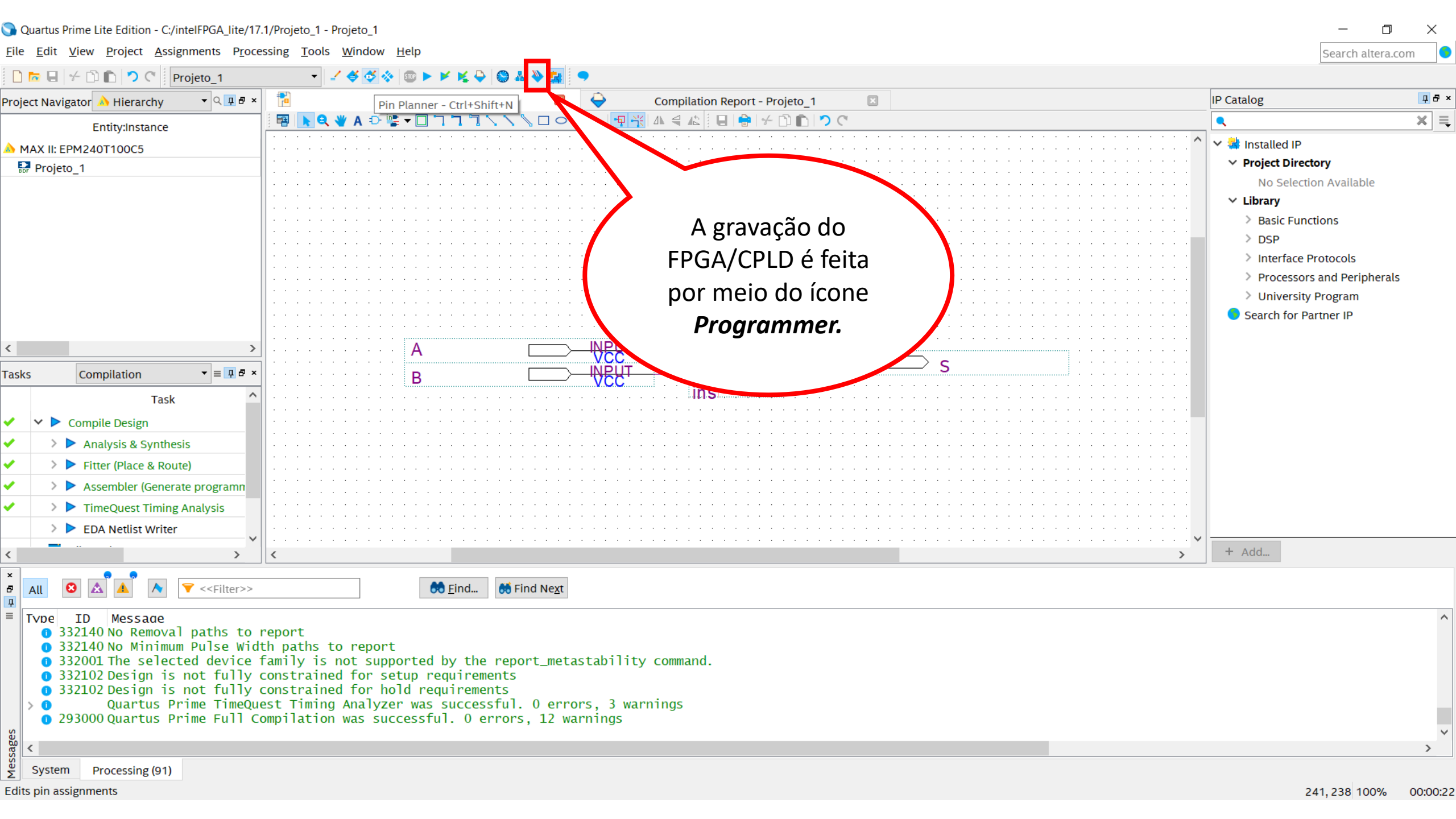
Properties:

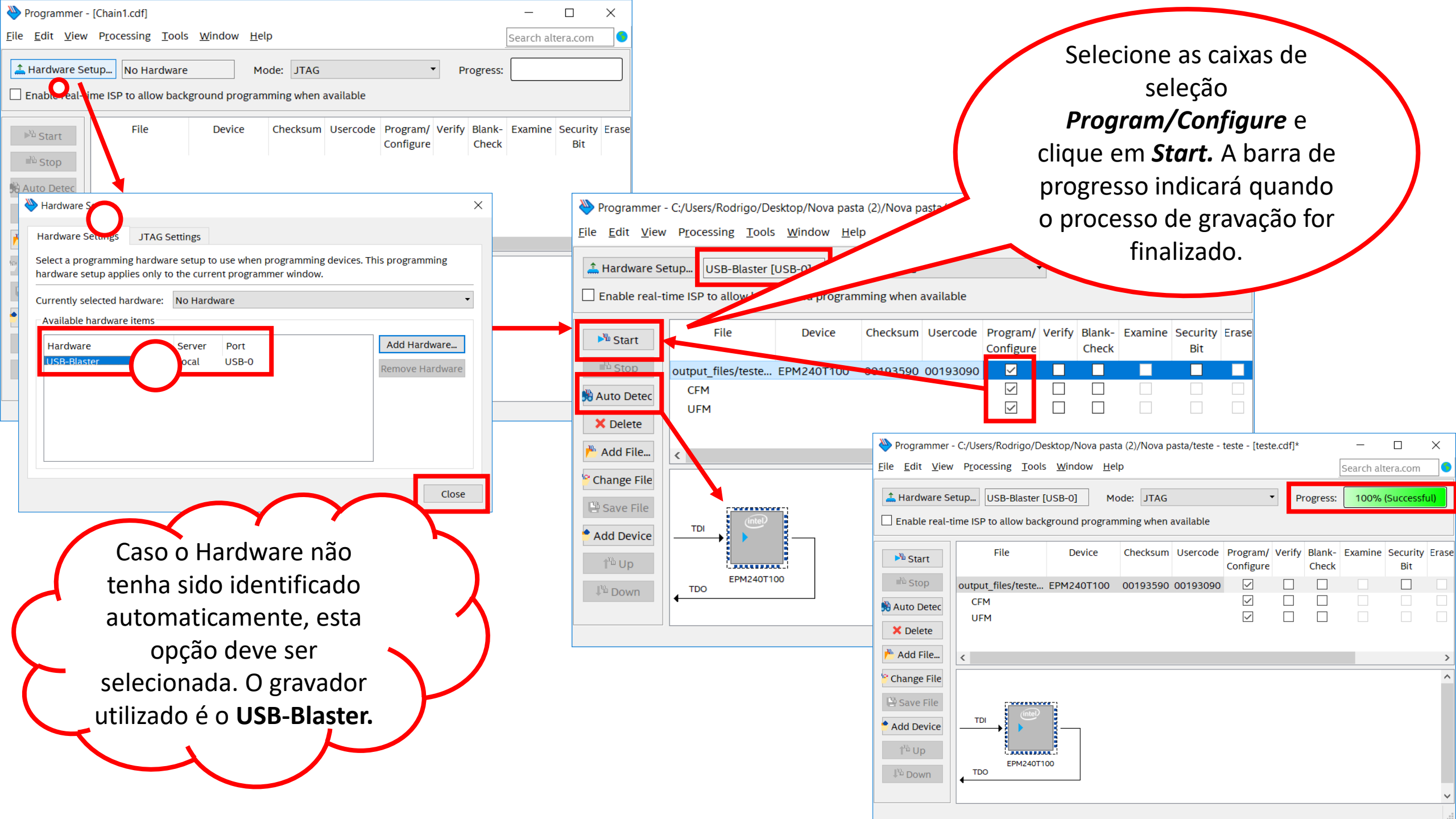
Named: * Filter: Pins: all

Node Name	Direction	Location	I/O Bank	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate Preservation
A	Input	PIN_75	2	PIN_8	3.3-V ...fault)		16mA ...ault)	
B	Input	PIN_76	2	PIN_12	3.3-V ...fault)		16mA ...ault)	
S	Output	PIN_77	2	PIN_7	3.3-V ...fault)		16mA ...ault)	
<<new node>>								

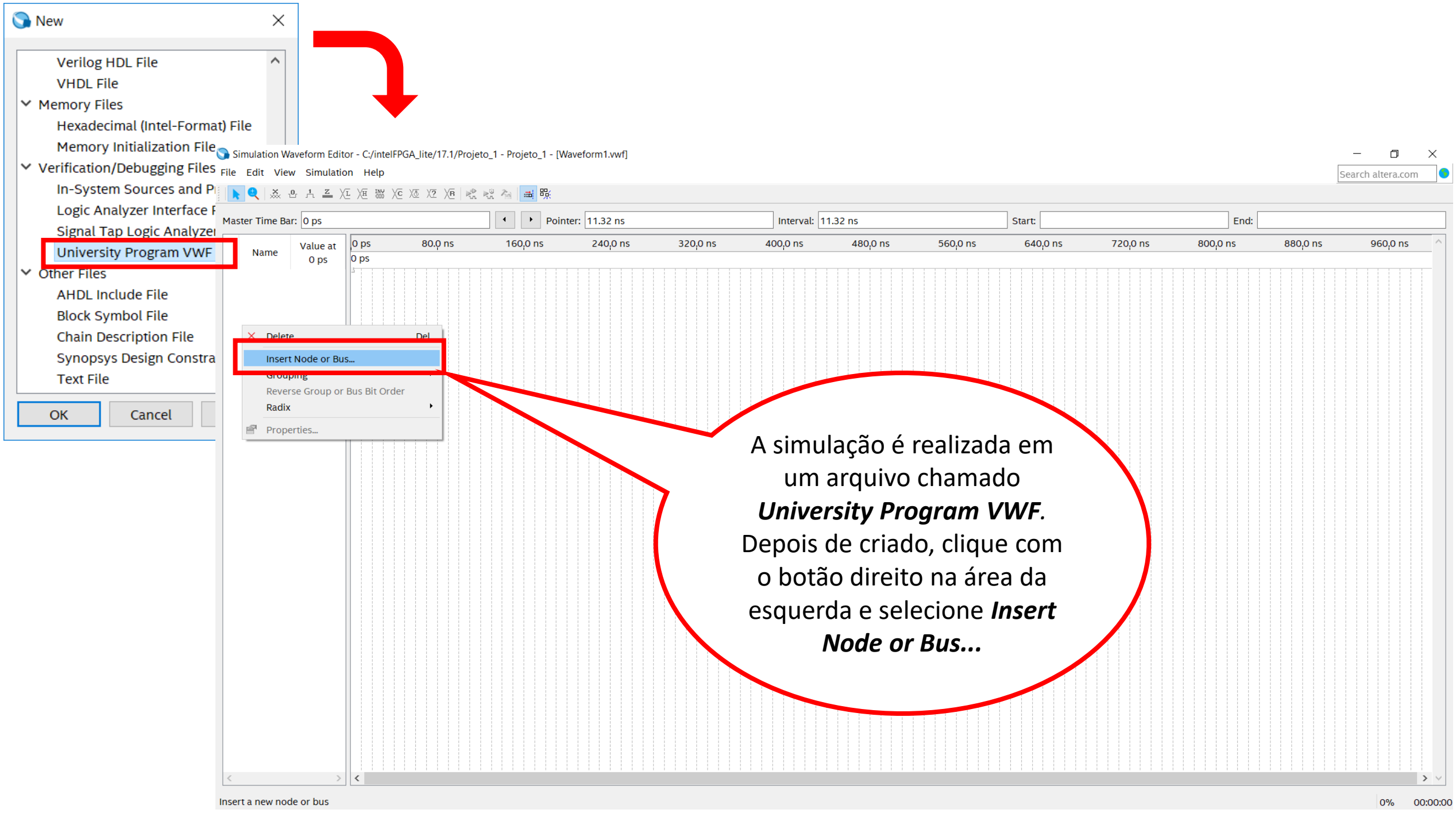
All Pins

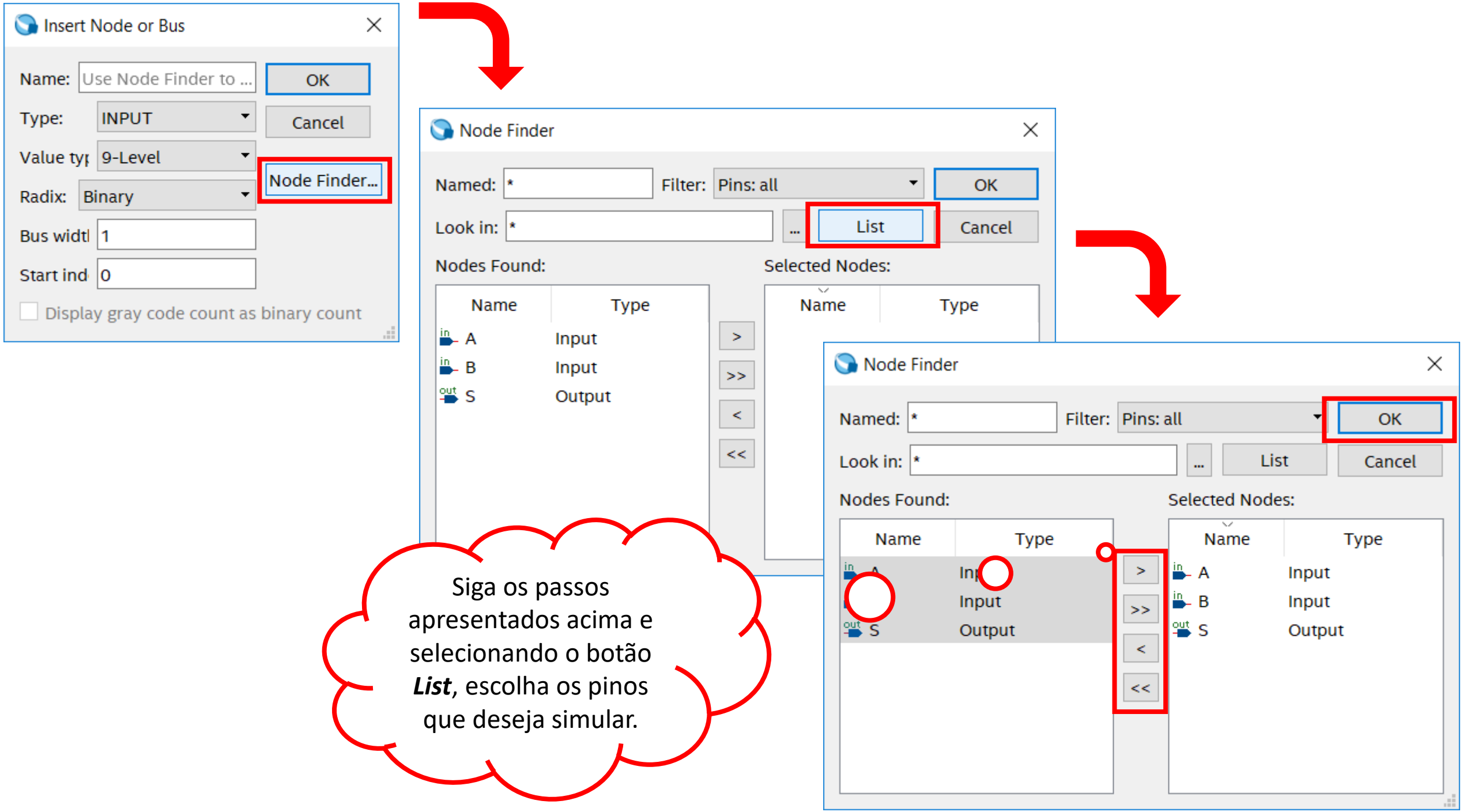
0% 00:00:00

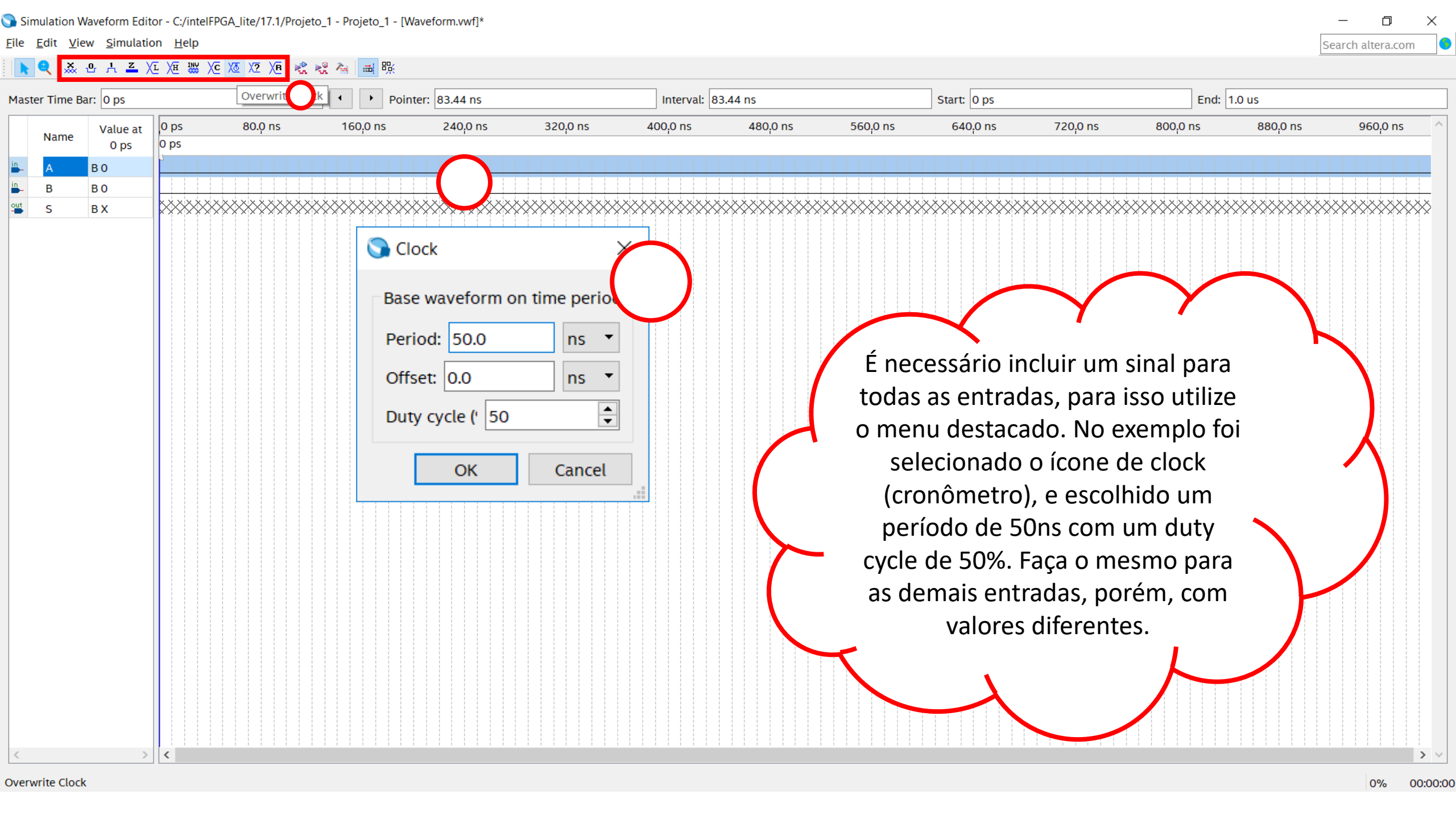

Quartus Prime Lite Edition - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Projeto_1
Pin Planner - Ctrl+Shift+N
Compilation Report - Projeto_1
Project Navigator Hierarchy
Entity:Instance
MAX II: EPM240T100C5
Projeto_1
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programn
TimeQuest Timing Analysis
EDA Netlist Writer
A gravação do FPGA/CPLD é feita por meio do ícone Programmer.
A
B
VCC
VCC
S
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
332140 No Removal paths to report
332140 No Minimum Pulse Width paths to report
332001 The selected device family is not supported by the report_metastability command.
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 3 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 12 warnings
Messages
System
Processing (91)
Edits pin assignments
241, 238 100%
00:00:22

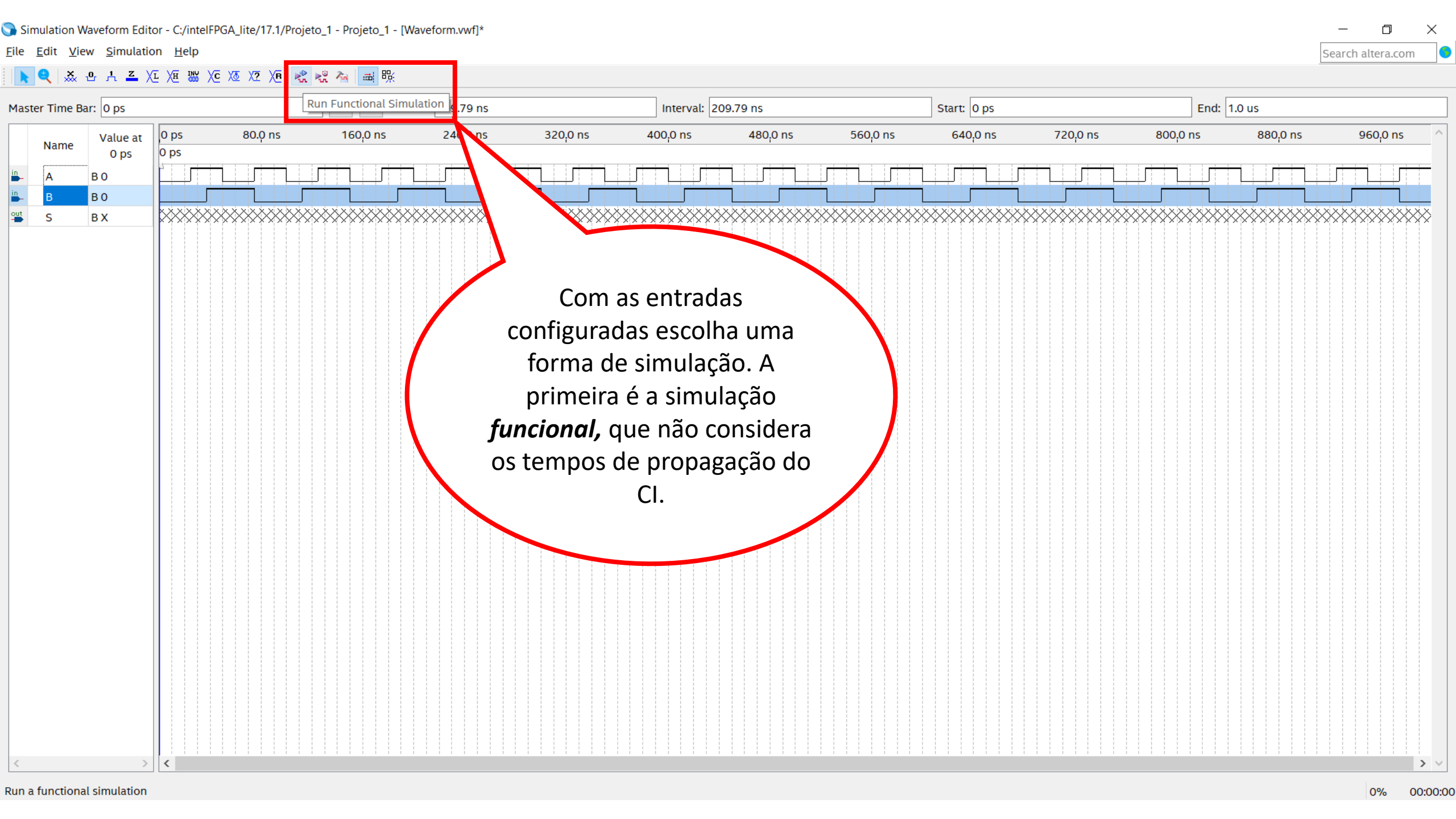

Programmer - [Chain1.cdf]
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
No Hardware
Mode: JTAG
Progress:
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detec
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
Erase
Hardware Settings
JTAG Settings
Select a programming hardware setup to use when programming devices. This programming hardware setup applies only to the current programmer window.
Currently selected hardware:
No Hardware
Available hardware items
Hardware
Server
Port
USB-Blaster
local
USB-0
Add Hardware...
Remove Hardware
Close
Programmer - C:/Users/Rodrigo/Desktop/Nova pasta (2)/Nova pasta
Hardware Setup...
USB-Blaster [USB-0]
Start
Stop
Auto Detec
Delete
Add File...
Change File
Save File
Add Device
Up
Down
output_files/teste...
EPM240T100
00193590
00193090
CFM
UFM
TDI
TDO
EPM240T100
Programmer - C:/Users/Rodrigo/Desktop/Nova pasta (2)/Nova pasta/teste - teste - [teste.cdf]*
Progress:
100% (Successful)
Selecione as caixas de seleção Program/Configure e clique em Start. A barra de progresso indicará quando o processo de gravação for finalizado.
Caso o Hardware não tenha sido identificado automaticamente, esta opção deve ser selecionada. O gravador utilizado é o USB-Blaster.

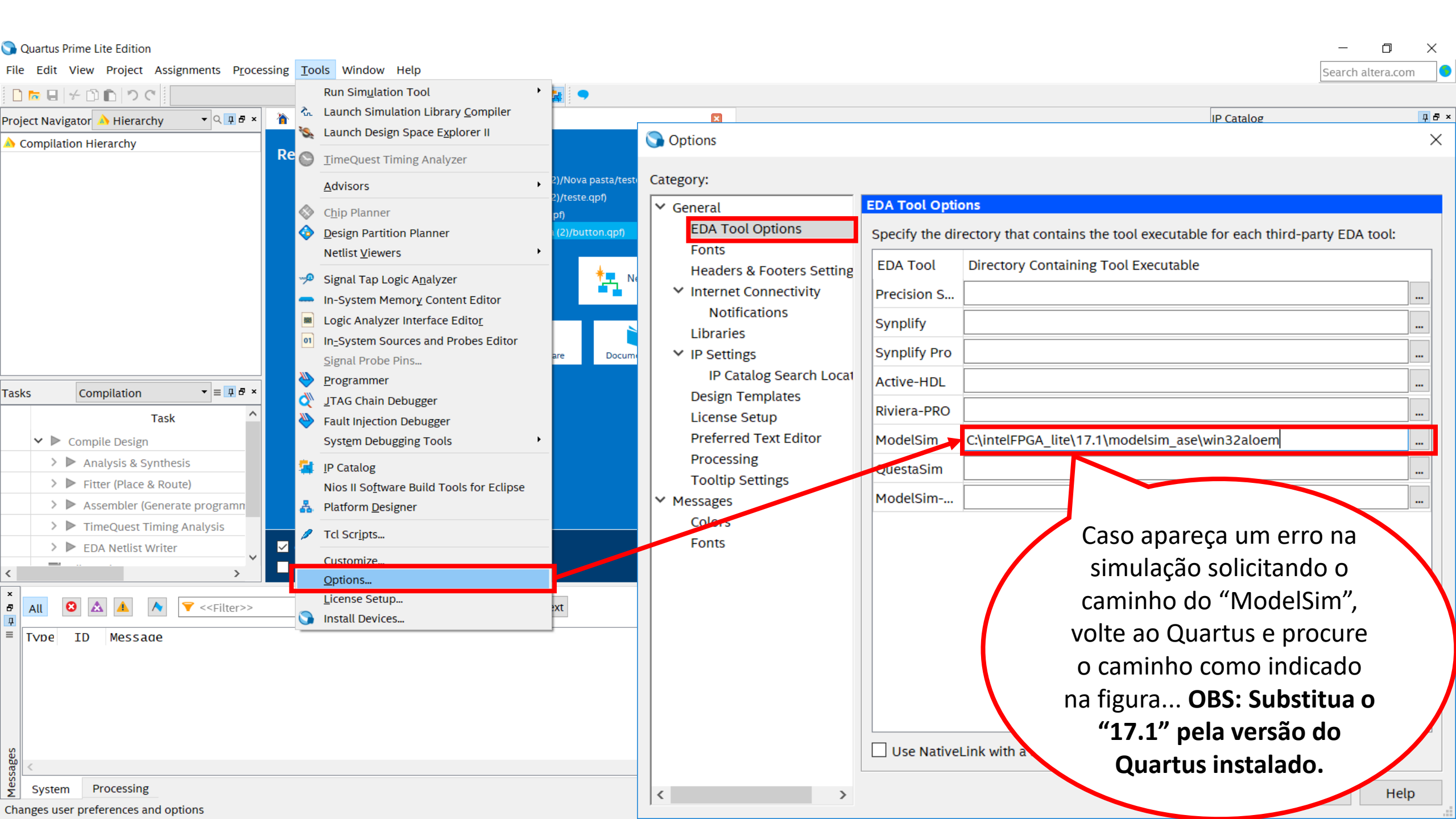
Simulação

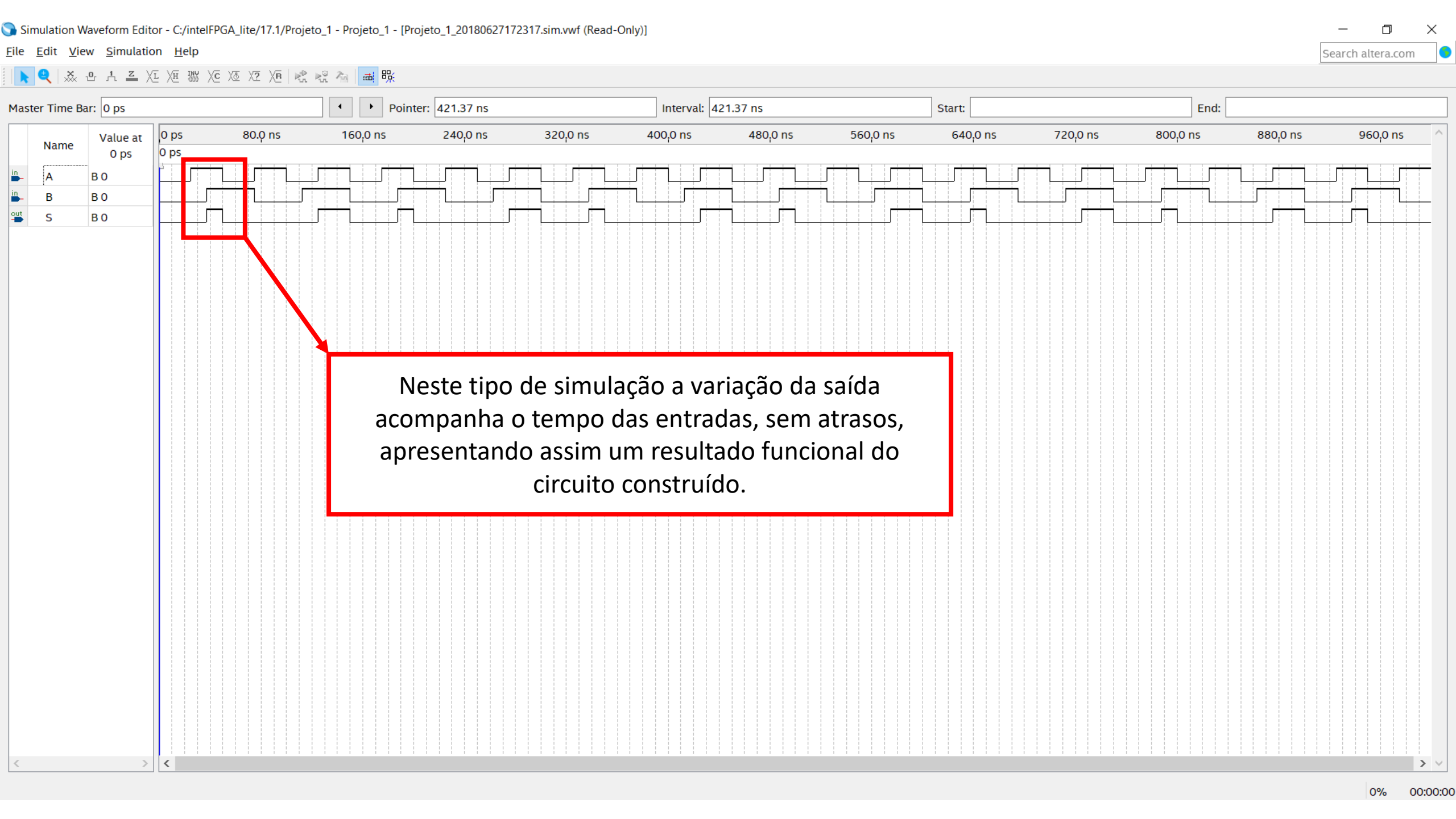

New
Verilog HDL File
VHDL File
Memory Files
Hexadecimal (Intel-Format) File
Memory Initialization File
Verification/Debugging Files
In-System Sources and P
Logic Analyzer Interface F
Signal Tap Logic Analyzer
University Program VWF
Other Files
AHDL Include File
Block Symbol File
Chain Description File
Synopsys Design Constra
Text File
OK
Cancel
Simulation Waveform Editor - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1 - [Waveform1.vwf]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 11.32 ns
Interval: 11.32 ns
Start:
End:
Name
Value at 0 ps
0 ps
80,0 ns
160,0 ns
240,0 ns
320,0 ns
400,0 ns
480,0 ns
560,0 ns
640,0 ns
720,0 ns
800,0 ns
880,0 ns
960,0 ns
Delete Del
Insert Node or Bus...
Grouping
Reverse Group or Bus Bit Order
Radix
Properties...
A simulação é realizada em um arquivo chamado University Program VWF. Depois de criado, clique com o botão direito na área da esquerda e selecione Insert Node or Bus...
Insert a new node or bus
0%
00:00:00

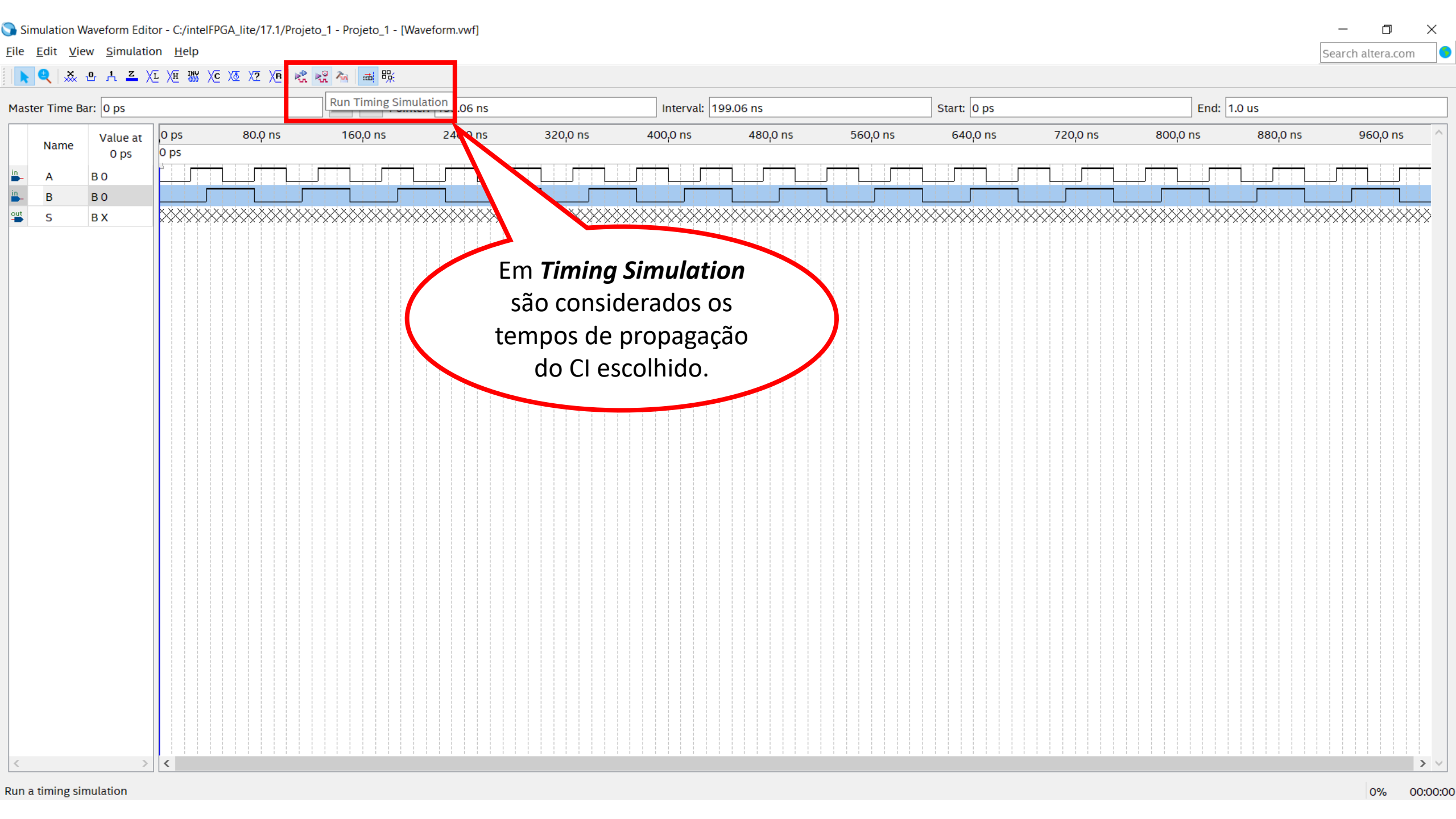

Insert Node or Bus
Name:
Use Node Finder to ...
OK
Type:
INPUT
Cancel
Value typ
9-Level
Node Finder...
Radix:
Binary
Bus widtl
1
Start ind
0
Display gray code count as binary count
Node Finder
Named:
*
Filter:
Pins: all
OK
Look in:
*
...
List
Cancel
Nodes Found:
Selected Nodes:
Name
Type
A
Input
B
Input
S
Output
>
>>
<
<<
Node Finder
Named:
*
Filter:
Pins: all
OK
Look in:
*
...
List
Cancel
Nodes Found:
Selected Nodes:
Name
Type
A
Input
B
Input
S
Output
>
>>
<
<<
Siga os passos apresentados acima e selecionando o botão ***List***, escolha os pinos que deseja simular.

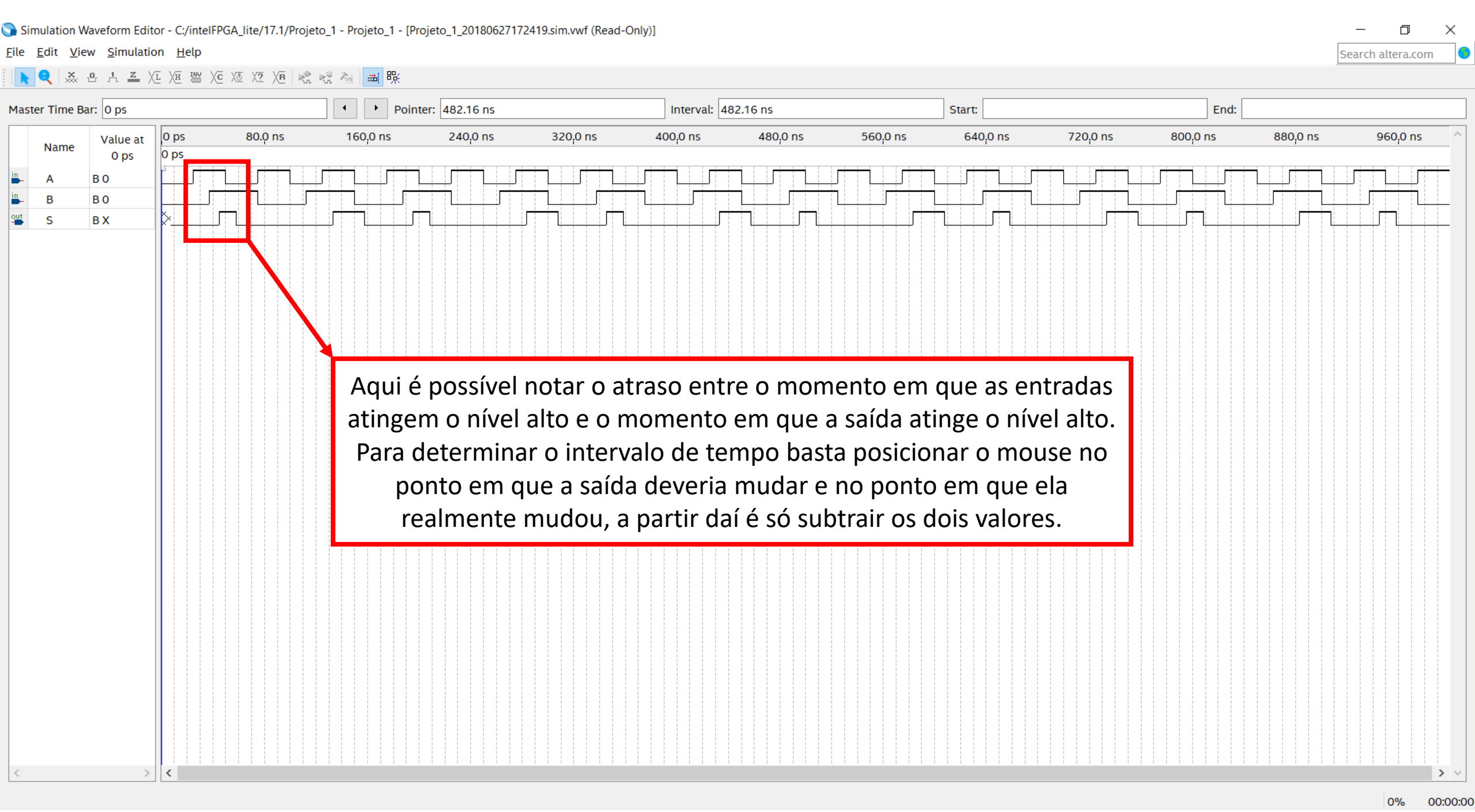

Simulation Waveform Editor - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1 - [Waveform.vwf]*
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 83.44 ns
Interval: 83.44 ns
Start: 0 ps
End: 1.0 us
Name
Value at 0 ps
A B 0
B B 0
S B X
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
Clock
Base waveform on time perio
Period: 50.0 ns
Offset: 0.0 ns
Duty cycle (' 50
OK
Cancel
É necessário incluir um sinal para todas as entradas, para isso utilize o menu destacado. No exemplo foi selecionado o ícone de clock (cronômetro), e escolhido um período de 50ns com um duty cycle de 50%. Faça o mesmo para as demais entradas, porém, com valores diferentes.
Overwrite Clock
0%
00:00:00


Simulation Waveform Editor - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1 - [Waveform.vwf]*
File Edit View Simulation Help
Search altera.com
Run Functional Simulation
Master Time Bar: 0 ps
Interval: 209.79 ns
Start: 0 ps
End: 1.0 us
Name
Value at 0 ps
A
B 0
B
B 0
S
B X
0 ps
80.0 ns
160.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
720.0 ns
800.0 ns
880.0 ns
960.0 ns
Com as entradas configuradas escolha uma forma de simulação. A primeira é a simulação ***funcional,*** que não considera os tempos de propagação do CI.
Run a functional simulation
0%
00:00:00

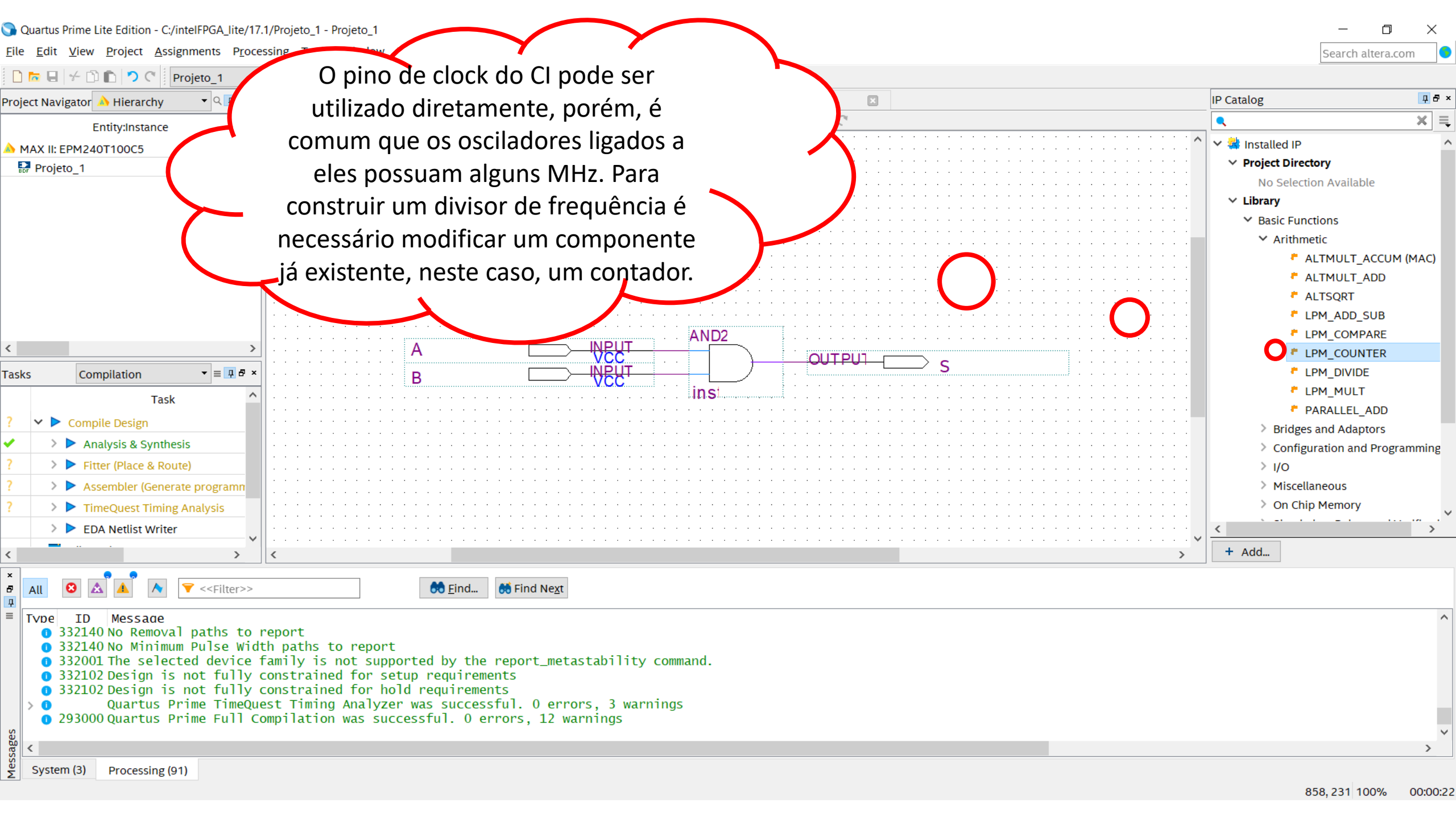

Quartus Prime Lite Edition
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Project Navigator Hierarchy
Compilation Hierarchy
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programn
TimeQuest Timing Analysis
EDA Netlist Writer
Run Simulation Tool
Launch Simulation Library Compiler
Launch Design Space Explorer II
TimeQuest Timing Analyzer
Advisors
Chip Planner
Design Partition Planner
Netlist Viewers
Signal Tap Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
Signal Probe Pins...
Programmer
JTAG Chain Debugger
Fault Injection Debugger
System Debugging Tools
IP Catalog
Nios II Software Build Tools for Eclipse
Platform Designer
Tcl Scripts...
Customize...
Options...
License Setup...
Install Devices...
IP Catalog
Options
Category:
General
EDA Tool Options
Fonts
Headers & Footers Setting
Internet Connectivity
Notifications
Libraries
IP Settings
IP Catalog Search Locat
Design Templates
License Setup
Preferred Text Editor
Processing
Tooltip Settings
Messages
Colors
Fonts
EDA Tool Options
Specify the directory that contains the tool executable for each third-party EDA tool:
EDA Tool
Directory Containing Tool Executable
Precision S...
Synplify
Synplify Pro
Active-HDL
Riviera-PRO
ModelSim
C:\intelFPGA_lite\17.1\modelsim_ase\win32aloem
QuestaSim
ModelSim-...
Use NativeLink with a
Help
All
<<Filter>>
Type ID Message
System Processing
Changes user preferences and options
Caso apareça um erro na simulação solicitando o caminho do “ModelSim”, volte ao Quartus e procure o caminho como indicado na figura... OBS: Substitua o “17.1” pela versão do Quartus instalado.

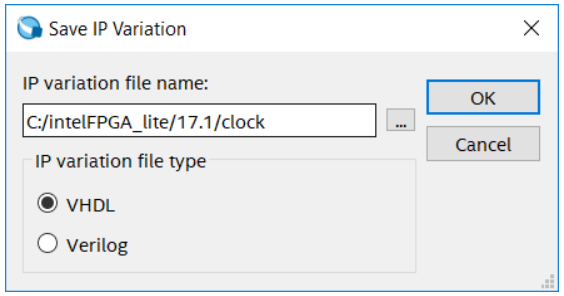

Simulation Waveform Editor - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1 - [Projeto_1_20180627172317.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 421.37 ns
Interval: 421.37 ns
Start:
End:
Name
Value at 0 ps
A B 0
B B 0
S B 0
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
720.0 ns
800.0 ns
880.0 ns
960.0 ns
Neste tipo de simulação a variação da saída acompanha o tempo das entradas, sem atrasos, apresentando assim um resultado funcional do circuito construído.
0%
00:00:00


Simulation Waveform Editor - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1 - [Waveform.vwf]
File Edit View Simulation Help
Search altera.com
Run Timing Simulation
Master Time Bar: 0 ps
Interval: 199.06 ns
Start: 0 ps
End: 1.0 us
Name
Value at 0 ps
A B 0
B B 0
S B X
0 ps
80.0 ns
160.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
720.0 ns
800.0 ns
880.0 ns
960.0 ns
Em *Timing Simulation* são considerados os tempos de propagação do CI escolhido.
Run a timing simulation
0%
00:00:00

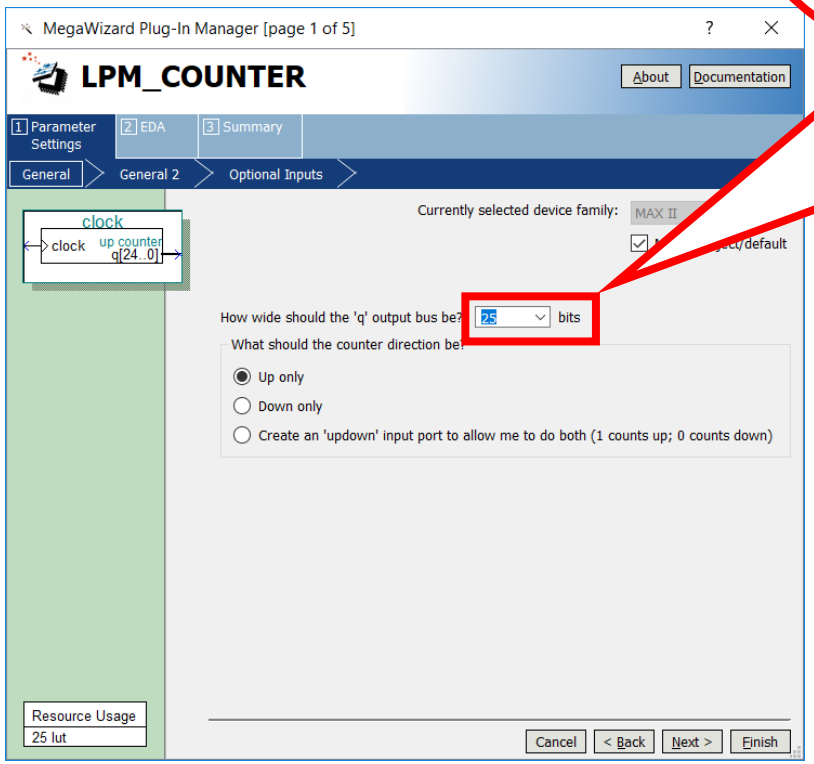

Simulation Waveform Editor - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1 - [Projeto_1_20180627172419.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 482.16 ns
Interval: 482.16 ns
Start:
End:
Name
Value at 0 ps
A B 0
B B 0
S B X
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
720.0 ns
800.0 ns
880.0 ns
960.0 ns
Aqui é possível notar o atraso entre o momento em que as entradas atingem o nível alto e o momento em que a saída atinge o nível alto. Para determinar o intervalo de tempo basta posicionar o mouse no ponto em que a saída deveria mudar e no ponto em que ela realmente mudou, a partir daí é só subtrair os dois valores.
0%
00:00:00

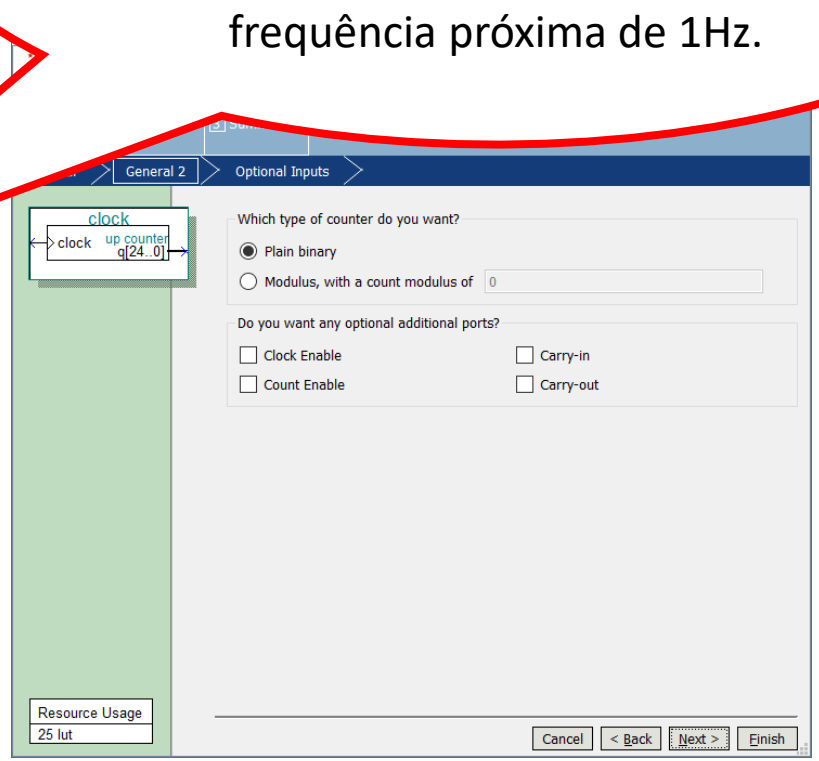
CLOCK

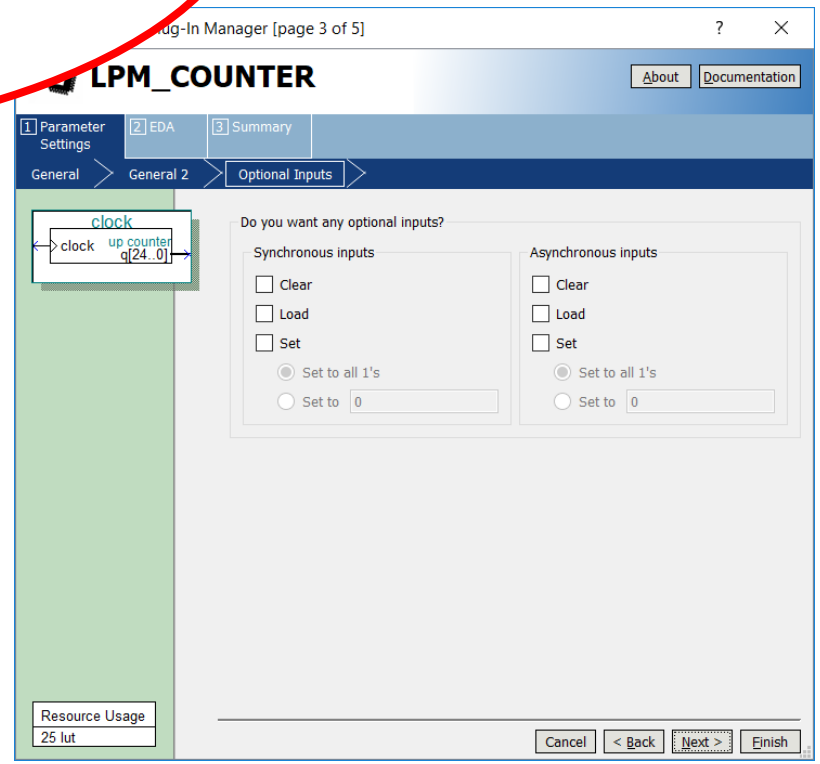

Quartus Prime Lite Edition - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1
File Edit View Project Assignments Processing
Search altera.com
Projeto_1
Project Navigator Hierarchy
Entity:Instance
MAX II: EPM240T100C5
Projeto_1
O pino de clock do CI pode ser utilizado diretamente, porém, é comum que os osciladores ligados a eles possuam alguns MHz. Para construir um divisor de frequência é necessário modificar um componente já existente, neste caso, um contador.
A
B
INPUT
VCC
INPUT
VCC
AND2
inst
OUTPUT
S
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
Arithmetic
ALTMULT_ACCUM (MAC)
ALTMULT_ADD
ALTSQRT
LPM_ADD_SUB
LPM_COMPARE
LPM_COUNTER
LPM_DIVIDE
LPM_MULT
PARALLEL_ADD
Bridges and Adaptors
Configuration and Programming
I/O
Miscellaneous
On Chip Memory
Add...
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programn
TimeQuest Timing Analysis
EDA Netlist Writer
All
<<Filter>>
Find...
Find Next
Type ID Message
332140 No Removal paths to report
332140 No Minimum Pulse Width paths to report
332001 The selected device family is not supported by the report_metastability command.
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 3 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 12 warnings
Messages
System (3)
Processing (91)
858, 231 100%
00:00:22

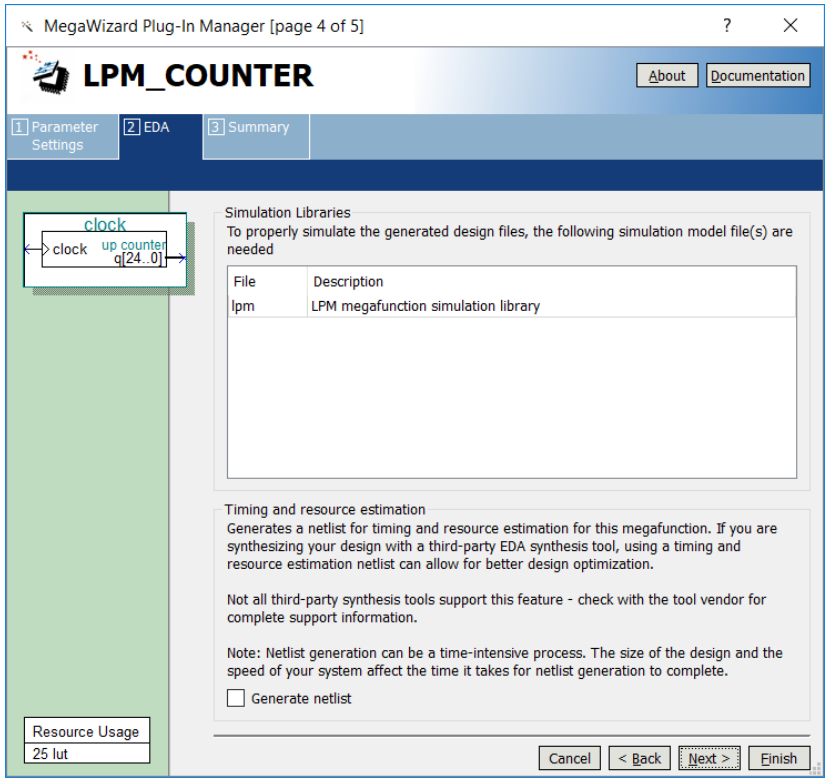


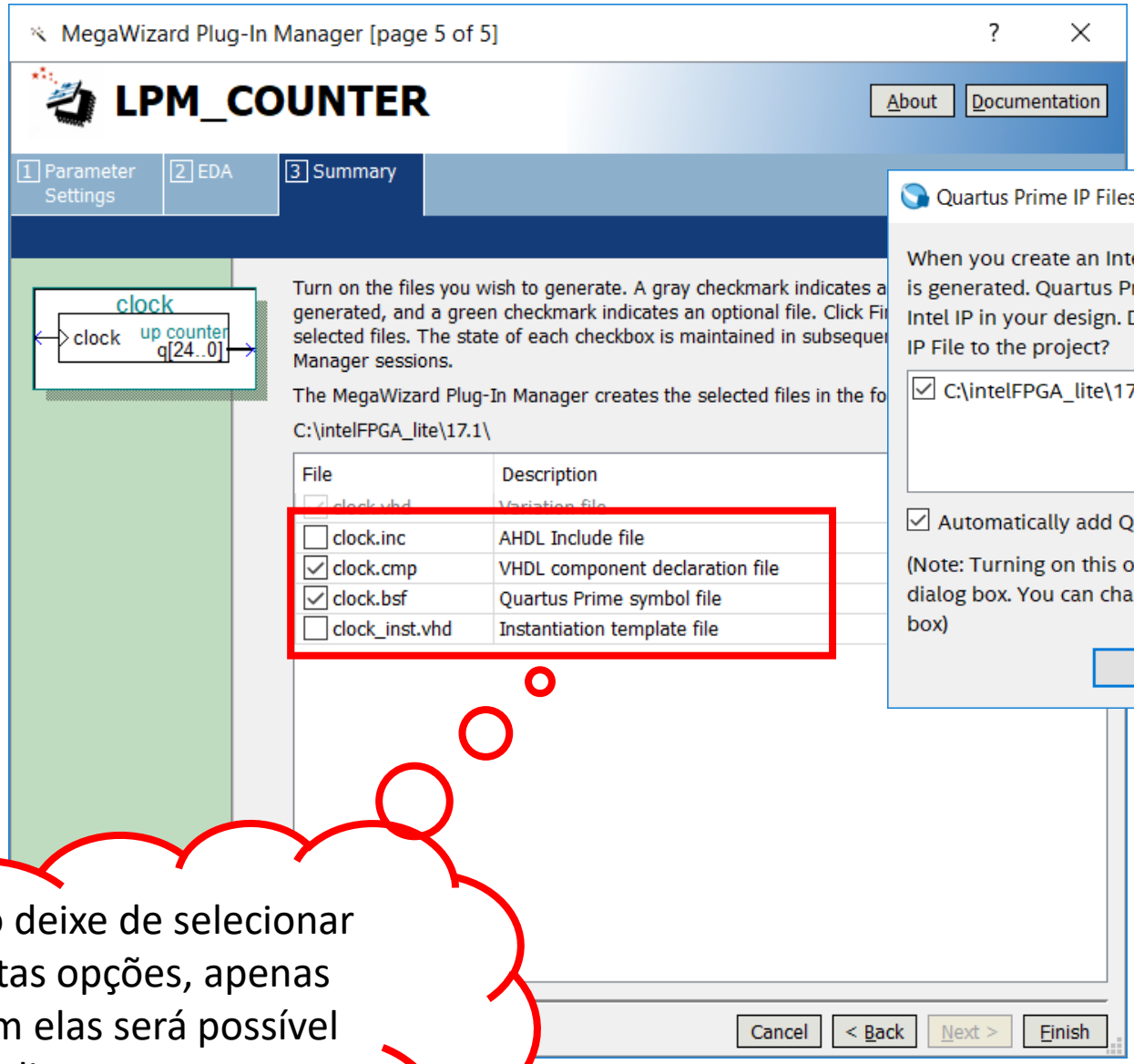
O número de bits necessários para o contador vai depender da mínima frequência desejada. Neste caso foi utilizado um clock de 50MHz, então o divisor deverá ter 25 bits para ter uma frequência próxima de 1Hz.

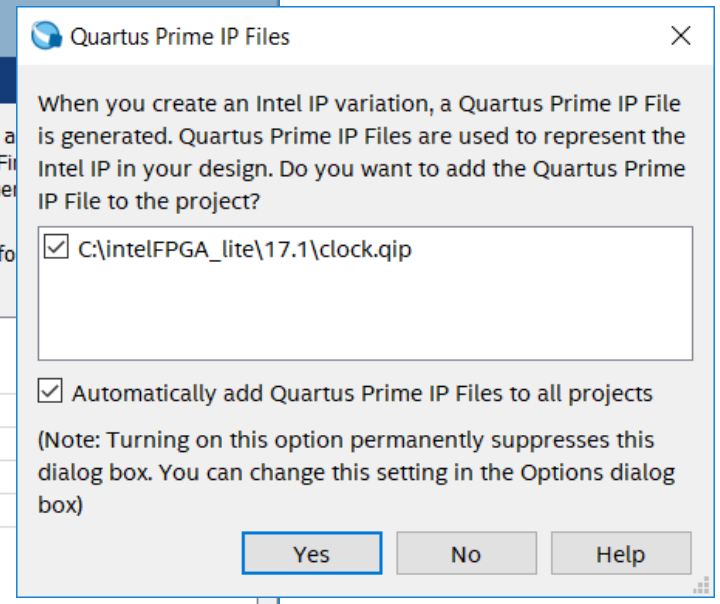




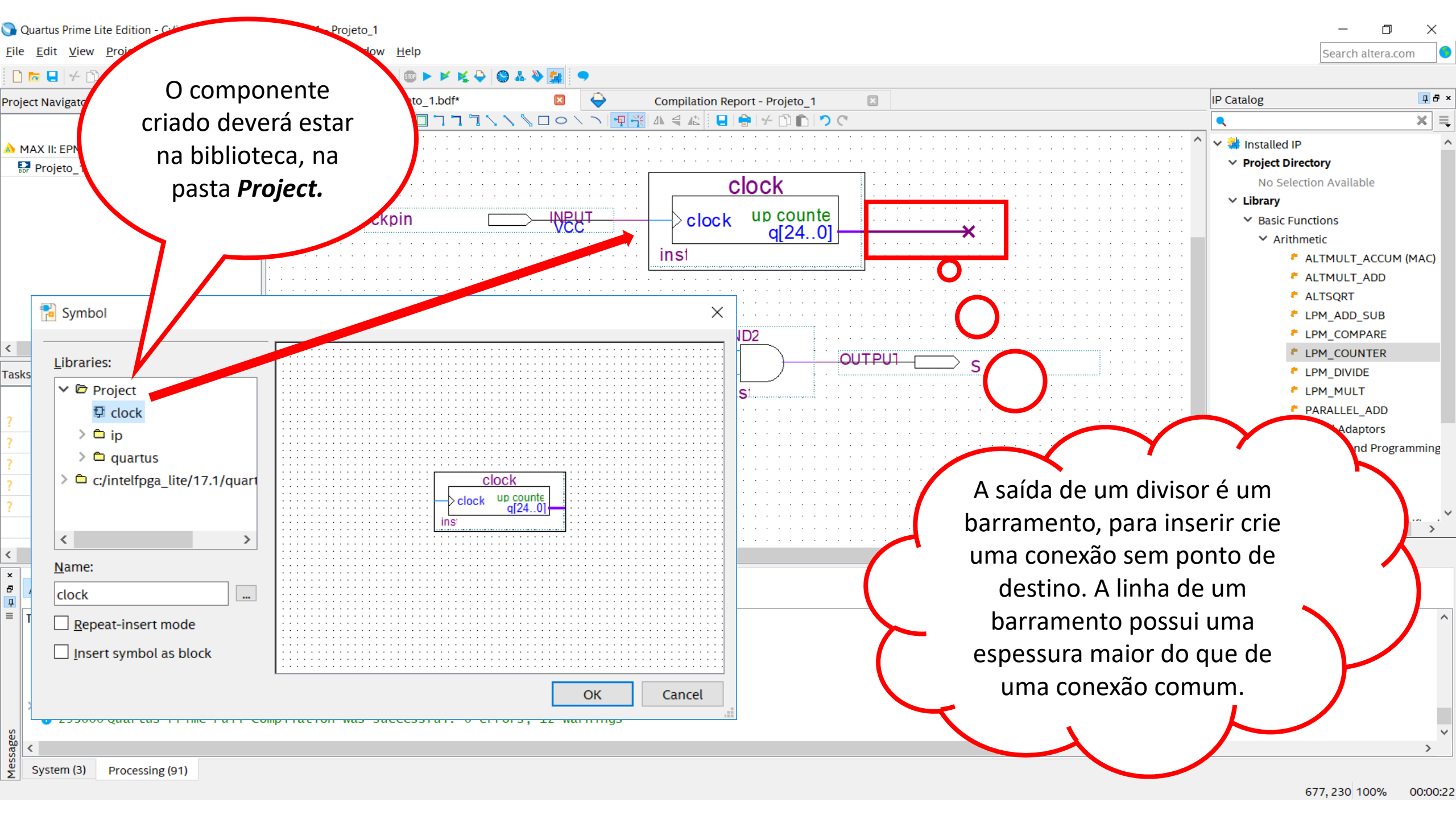


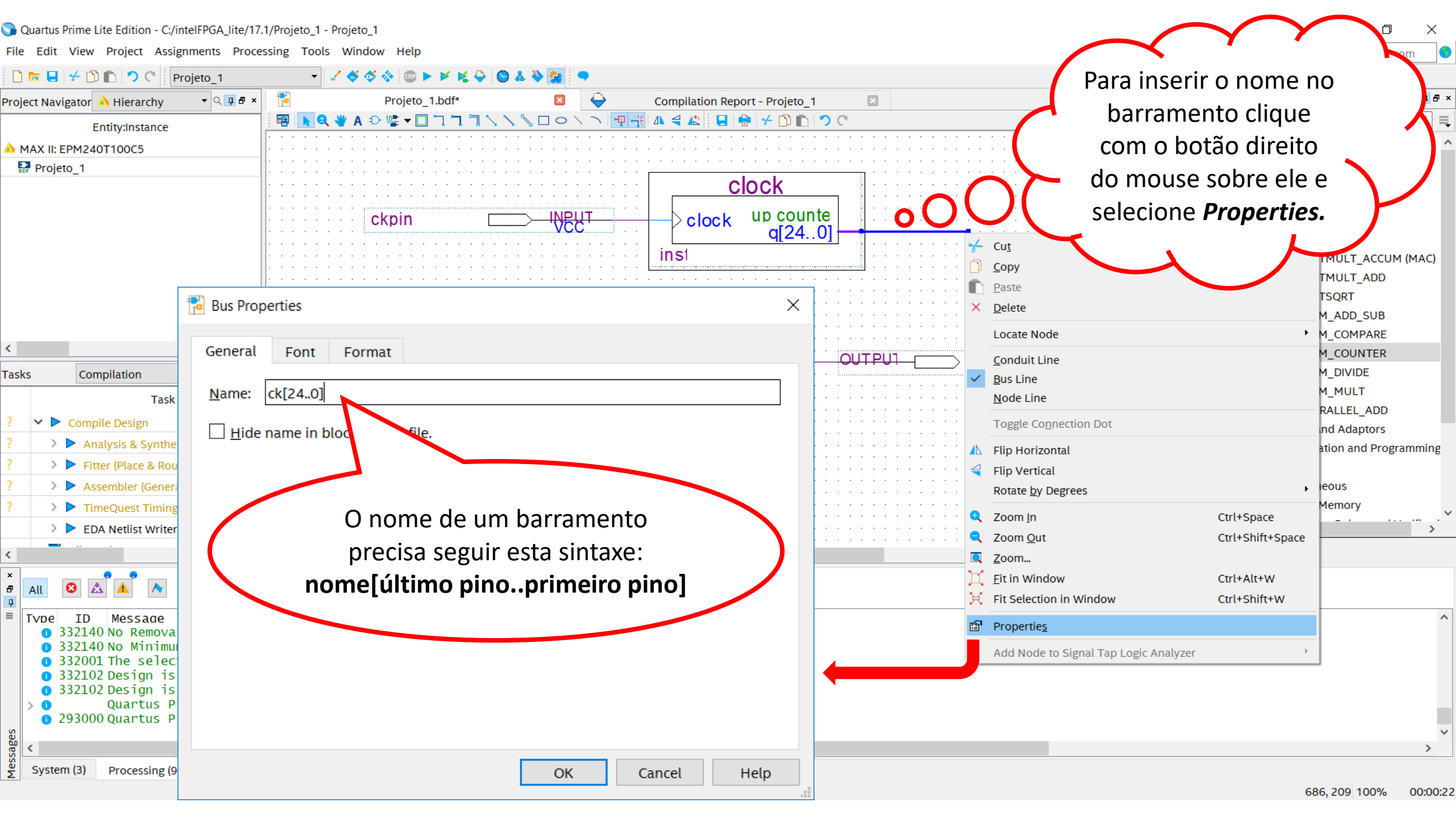


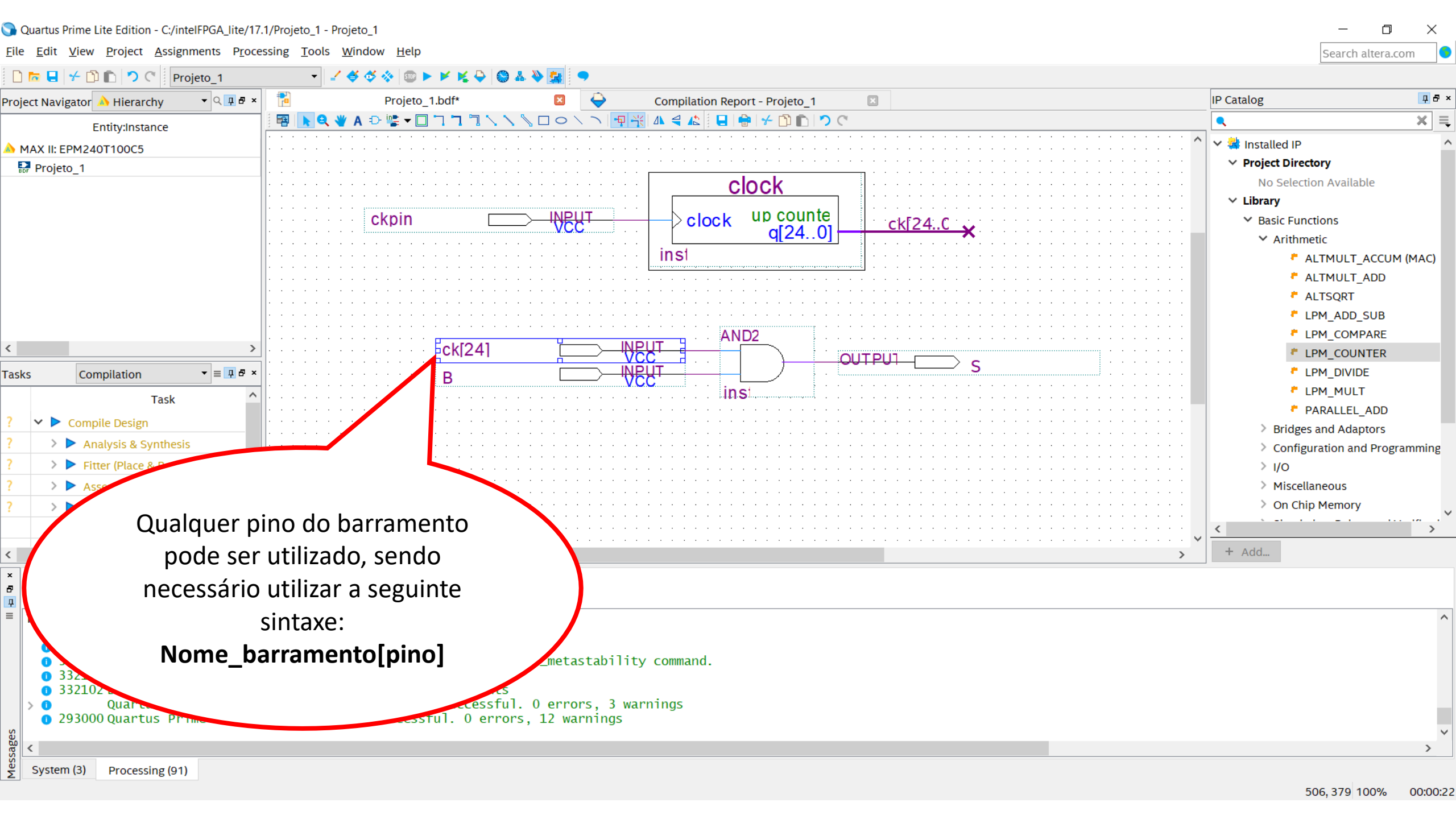




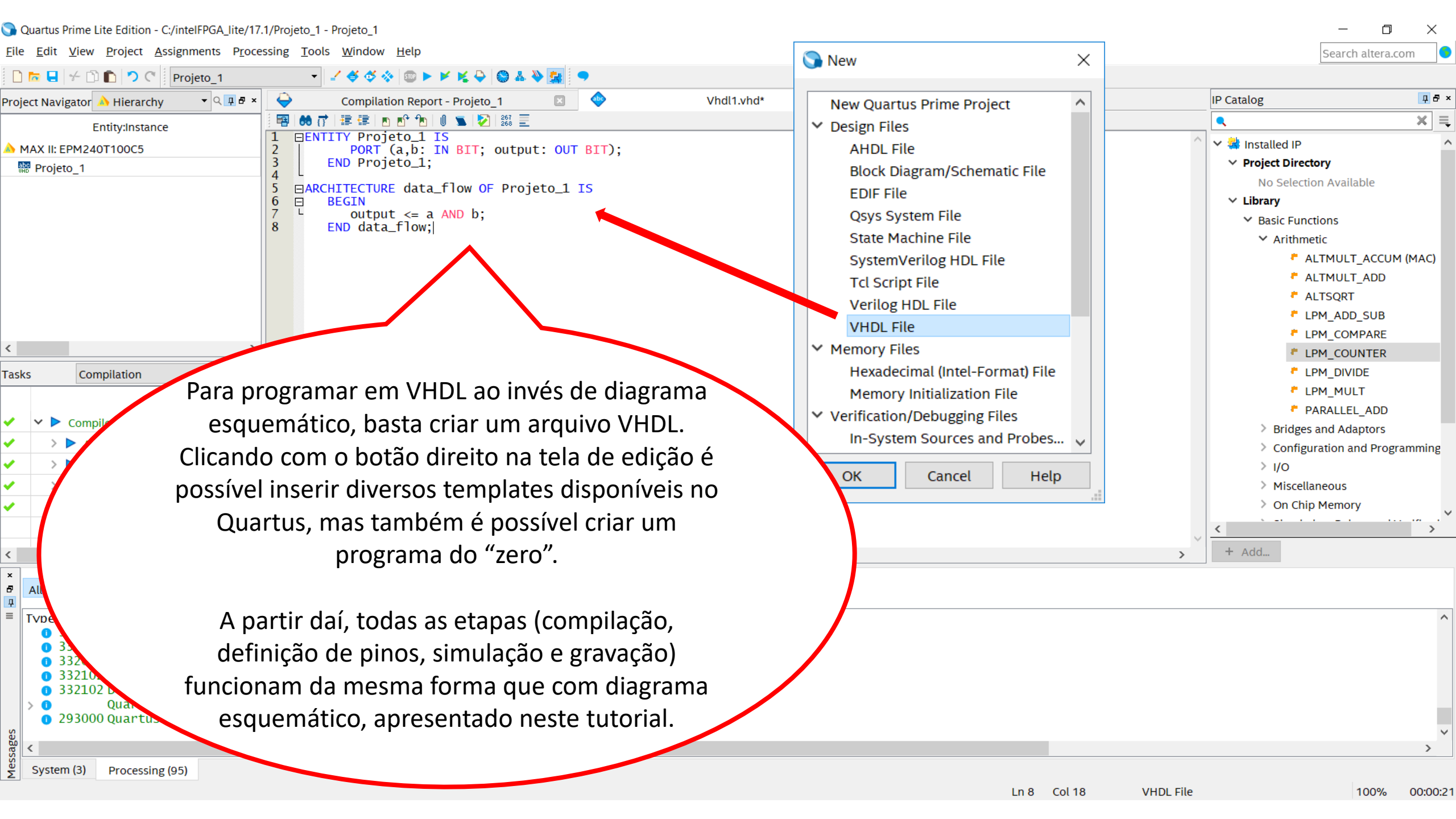
Não deixe de selecionar estas opções, apenas com elas será possível visualizar o componente no esquemático.


O componente criado deverá estar na biblioteca, na pasta *Project.*
Symbol
Libraries:
Project
clock
ip
quartus
c:/intelfpga_lite/17.1/quart
Name:
clock
Repeat-insert mode
Insert symbol as block
OK
Cancel
clock
up counte
q[24..0]
INPUT
VCC
OUTPUT
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
Arithmetic
ALTMULT_ACCUM (MAC)
ALTMULT_ADD
ALTSQRT
LPM_ADD_SUB
LPM_COMPARE
LPM_COUNTER
LPM_DIVIDE
LPM_MULT
PARALLEL_ADD
A saída de um divisor é um barramento, para inserir crie uma conexão sem ponto de destino. A linha de um barramento possui uma espessura maior do que de uma conexão comum.


Quartus Prime Lite Edition - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1
File Edit View Project Assignments Processing Tools Window Help
Projeto_1
Project Navigator Hierarchy
Entity:Instance
MAX II: EPM240T100C5
Projeto_1
Projeto_1.bdf*
Compilation Report - Projeto_1
clock
ckpin
INPUT
VCC
clock
up counte
q[24..0]
inst
OUTPUT
Para inserir o nome no barramento clique com o botão direito do mouse sobre ele e selecione Properties.
Cut
Copy
Paste
Delete
Locate Node
Conduit Line
Bus Line
Node Line
Toggle Connection Dot
Flip Horizontal
Flip Vertical
Rotate by Degrees
Zoom In Ctrl+Space
Zoom Out Ctrl+Shift+Space
Zoom...
Fit in Window Ctrl+Alt+W
Fit Selection in Window Ctrl+Shift+W
Properties
Add Node to Signal Tap Logic Analyzer
Bus Properties
General
Font
Format
Name: ck[24..0]
Hide name in bloc file.
O nome de um barramento precisa seguir esta sintaxe:
nome[último pino..primeiro pino]
OK
Cancel
Help
Tasks
Compilation
Compile Design
Analysis & Synthe
Fitter (Place & Rou
Assembler (Genera
TimeQuest Timing
EDA Netlist Writer
Type ID Message
332140 No Removal
332140 No Minimu
332001 The selec
332102 Design is
332102 Design is
Quartus P
293000 Quartus P
System (3)
Processing (9
Messages
686, 209 100% 00:00:22


Quartus Prime Lite Edition - C:/intelFPGA_lite/17.1/Projeto_1 - Projeto_1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Projeto_1
Project Navigator Hierarchy
Entity:Instance
MAX II: EPM240T100C5
Projeto_1
Projeto_1.bdf*
Compilation Report - Projeto_1
clock
ckpin
INPUT
VCC
clock
up counte
q[24..0]
ck[24..0
inst
ck[24]
B
INPUT
VCC
INPUT
VCC
AND2
OUTPUT
S
inst
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
Arithmetic
ALTMULT_ACCUM (MAC)
ALTMULT_ADD
ALTSQRT
LPM_ADD_SUB
LPM_COMPARE
LPM_COUNTER
LPM_DIVIDE
LPM_MULT
PARALLEL_ADD
Bridges and Adaptors
Configuration and Programming
I/O
Miscellaneous
On Chip Memory
Add...
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place &
Qualquer pino do barramento pode ser utilizado, sendo necessário utilizar a seguinte sintaxe:
Nome_barramento[pino]
metastability command.
293000 Quartus
ccessful. 0 errors, 12 warnings
Messages
System (3)
Processing (91)
506, 379 100%
00:00:22

VHDL

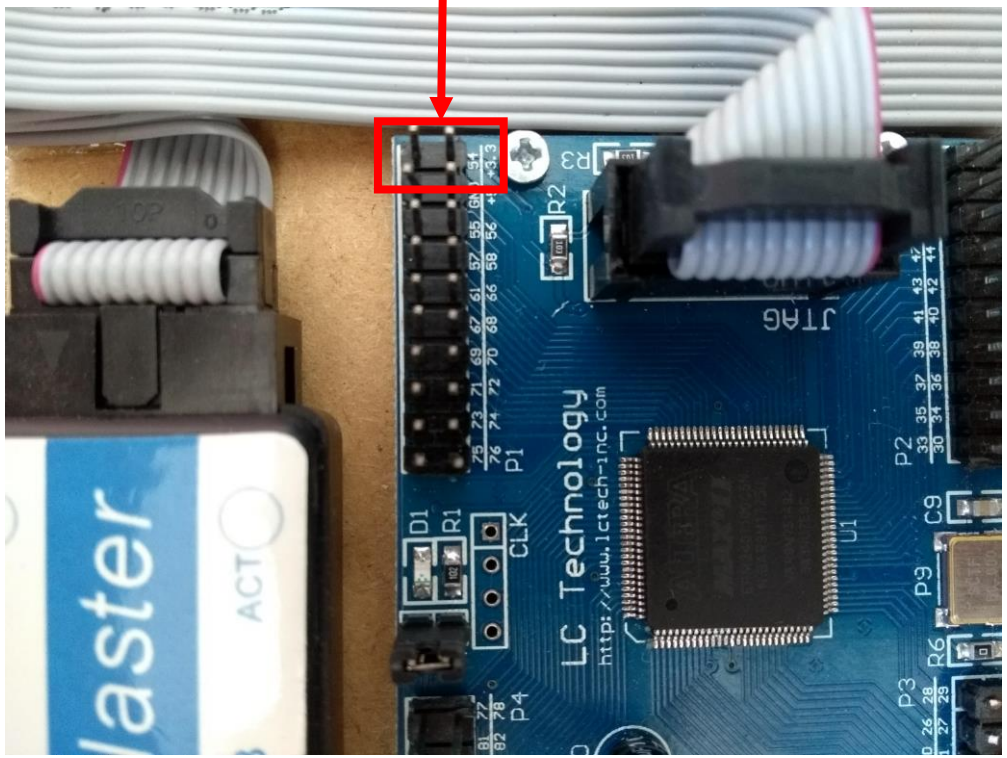


Para programar em VHDL ao invés de diagrama esquemático, basta criar um arquivo VHDL. Clicando com o botão direito na tela de edição é possível inserir diversos templates disponíveis no Quartus, mas também é possível criar um programa do “zero”.

A partir daí, todas as etapas (compilação, definição de pinos, simulação e gravação) funcionam da mesma forma que com diagrama esquemático, apresentado neste tutorial.

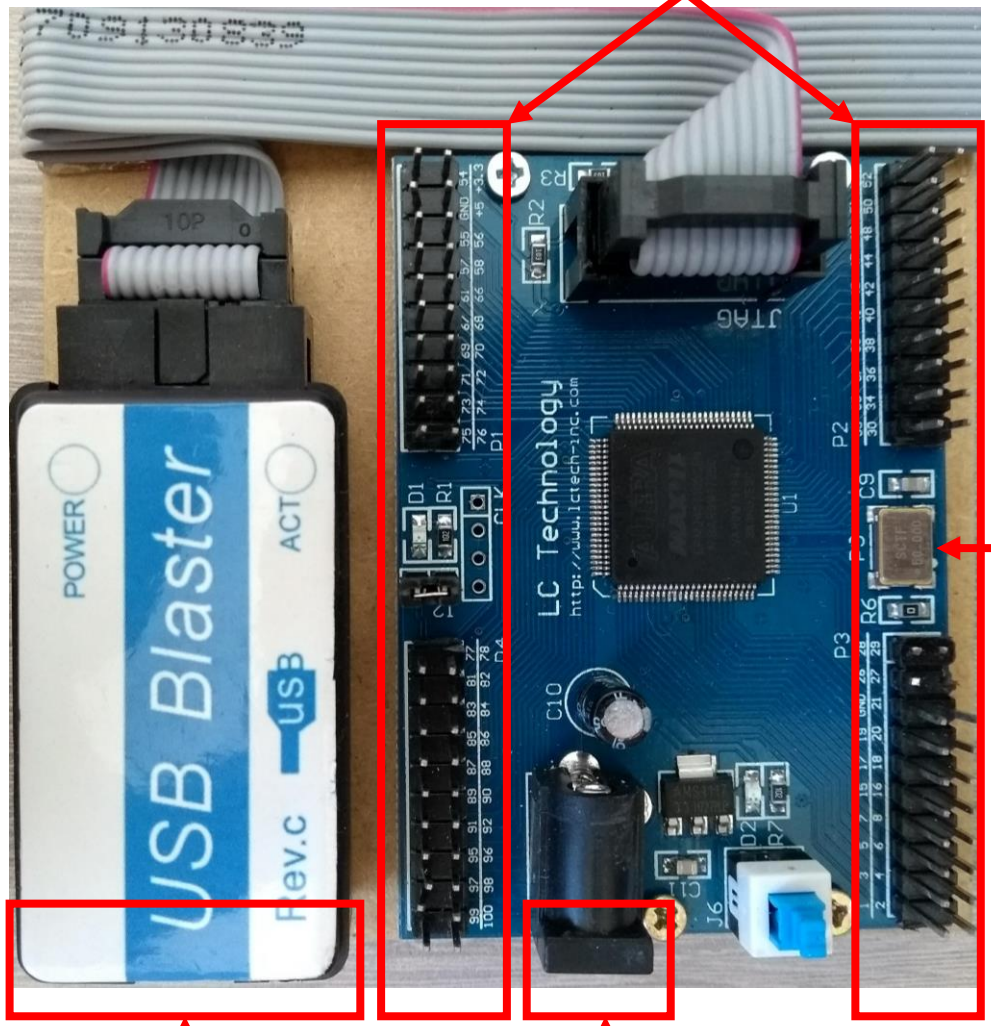
Pinagem das placas

Pinos de alimentação.
GND, 5V e 3,3V



OBS: A alimentação dos pinos é retirada da porta USB e não existe nenhuma proteção na placa. Tome cuidado ao utilizá-los em algum circuito.

I/Os disponíveis.
Tensão – 3,3V

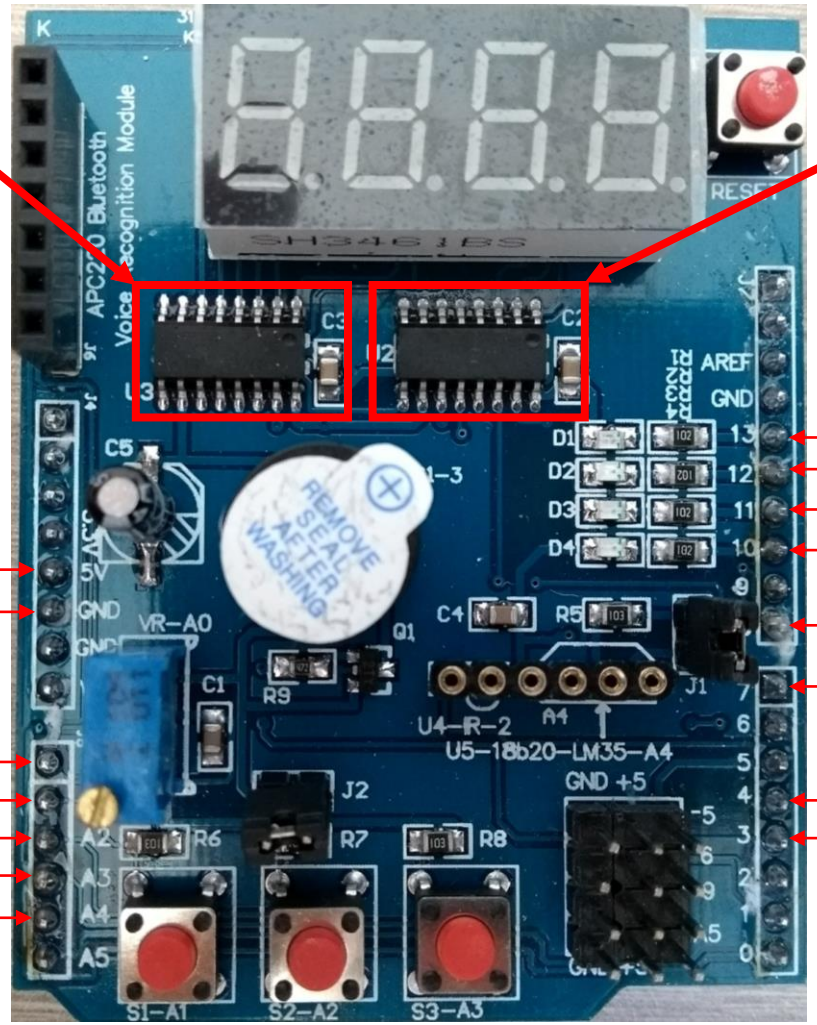


Cristal de 50MHz.
Pino 12

Gravador USB-Blaster.

Alimentação 5V

Placa de expansão. O esquema eletrônico se encontra na próxima página...



Esquema eletrônico da placa de expansão.